Spartan-6 FPGA Data Sheet: DC and Switching Characteristics

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Advance Product Specification

Spartan-6 FPGA Electrical Characteristics

Spartan®-6 LX FPGAs are available in -3, -2, and -1L speed grades, with -3 having the highest performance. Spartan-6 LXT FPGAs are available in -4, -3, and -2 speed grades, with -4 having the highest performance. Spartan-6 FPGA DC and AC characteristics are specified for both commercial and industrial grades. Except the operating temperature range or unless otherwise noted, all the DC and AC electrical parameters are the same for a particular speed grade (that is, the timing characteristics of a -2 speed grade industrial device are the same as for a -2 speed grade commercial device). However, only selected speed grades and/or devices might be available in the industrial range.

All supply voltage and junction temperature specifications are representative of worst-case conditions. The parameters included are common to popular designs and typical applications.

This Spartan-6 FPGA data sheet, part of an overall set of documentation on the Spartan-6 family of FPGAs, is available on the Xilinx website.

All specifications are subject to change without notice.

Spartan-6 FPGA DC Characteristics

Table 1: **Absolute Maximum Ratings(1)**

Symbol	Description		Units
V_{CCINT}	Internal supply voltage relative to GND	–0.5 to 1.32	V
V_{CCAUX}	Auxiliary supply voltage relative to GND	–0.5 to 3.75	V
V_{CCO}	Output drivers supply voltage relative to GND	–0.5 to 3.75	V
V_{BATT}	Key memory battery backup supply (XC6SLX75, XC6SLX75T, XC6SLX100, XC6SLX100T, XC6SLX150, and XC6SLX150T only)	–0.5 to 4.05	V
V_{FS}	External voltage supply for eFUSE programming (XC6SLX75, XC6SLX75T, XC6SLX100, XC6SLX100T, XC6SLX150, and XC6SLX150T only).(2)	–0.5 to 3.75	V
V_{REF}	Input reference voltage	–0.5 to 3.75	V
V_{IN}(3)	I/O input voltage relative to GND(4) (user and dedicated I/Os)	–0.95 to 4.1	V
V_{TS}	Voltage applied to 3-state output (user and dedicated I/Os)	–0.95 to 4.1	V
T_{STG}	Storage temperature (ambient)	–65 to 150	°C
T_{SOL}	Maximum soldering temperature(5) (TQG144, CPG196, CSG225, CSG324, CSG484, and FTG256)	+260	°C
	Maximum soldering temperature(5) (Pb-free packages: FGG484, FGG676, and FGG900)	+250	°C
	Maximum soldering temperature(5) (Pb packages: FT256, FG484, FG676, and FG900)	+220	°C
T_j	Maximum junction temperature(5)	+125	°C

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
2. When programming eFUSE, $V_{FS} \leq V_{CCAUX}$. Requires up to 40 mA current. For read mode, V_{FS} can be between GND and 3.45 V.
3. I/O absolute maximum limit applied to DC and AC signals.
4. For I/O operation, refer to the *Spartan-6 FPGA SelectIO Resources User Guide.*
5. For soldering guidelines and thermal considerations, see *Spartan-6 FPGA Packaging and Pinout Specification*.

Table 2: **Recommended Operating Conditions(1)**

Symbol	Description	Temperature Range	Speed Grade	Min	Typ	Max	Units
V_{CCINT}	Internal supply voltage relative to GND, T_j = 0°C to +85°C	Commercial	-4, -3, -2	1.14	1.2	1.26	V
			-1L	0.95	1.0	1.05	V
	Internal supply voltage relative to GND, T_j = –40°C to +100°C	Industrial	-3, -2	1.14	1.2	1.26	V
			-1L	0.95	1.0	1.05	V
V_{CCAUX}(2)	Auxiliary supply voltage relative to GND when V_{CCAUX} = 2.5V, T_j = 0°C to +85°C	Commercial	-4, -3, -2, -1L	2.375	2.5	2.625	V
	Auxiliary supply voltage relative to GND when V_{CCAUX} = 2.5V, T_j = –40°C to +100°C	Industrial	-3, -2, -1L				
	Auxiliary supply voltage relative to GND when V_{CCAUX} = 3.3V, T_j = 0°C to +85°C	Commercial	-4, -3, -2, -1L	3.15	3.3	3.45	V
	Auxiliary supply voltage relative to GND when V_{CCAUX} = 3.3V, T_j = –40°C to +100°C	Industrial	-3, -2, -1L				
V_{CCO}(3, 4)	Output supply voltage relative to GND, T_j = 0°C to +85°C	Commercial	-4, -3, -2, -1L	1.1	–	3.45	V
	Output supply voltage relative to GND, T_j = –40°C to +100°C	Industrial	-3, -2, -1L				
V_{IN}	Input voltage relative to GND, T_j = 0°C to +85°C	Commercial	-4, -3, -2, -1L	–0.5	–	4.0	V
	Input voltage relative to GND, T_j = –40°C to +100°C	Industrial	-3, -2, -1L	–0.5	–	3.95	V
	Input voltage relative to GND, PCI I/O standard, T_j = 0°C to +85°C	Commercial	-4, -3, -2, -1L	–0.5	–	V_{CCO} + 0.5	V
	Input voltage relative to GND, PCI I/O standard, T_j = –40°C to +100°C	Industrial	-3, -2, -1L	–0.5	–	V_{CCO} + 0.5	V
I_{IN}(5)	Maximum current through pin using PCI I/O standard when forward biasing the clamp diode.	Commercial	-4, -3, -2, -1L	–	–	10	mA
		Industrial	-3, -2, -1L	–	–	10	mA
V_{BATT}(6)	Battery voltage relative to GND, T_j = 0°C to +85°C (XC6SLX75, XC6SLX75T, XC6SLX100, XC6SLX100T, XC6SLX150, and XC6SLX150T only)	Commercial	-4, -3, -2, -1L	1.0	–	3.6	V
	Battery voltage relative to GND, T_j = –40°C to +100°C (XC6SLX75, XC6SLX75T, XC6SLX100, XC6SLX100T, XC6SLX150, and XC6SLX150T only)	Industrial	-3, -2, -1L				
V_{FS}(7)	External voltage supply for eFUSE programming (XC6SLX75, XC6SLX75T, XC6SLX100, XC6SLX100T, XC6SLX150, and XC6SLX150T only).	All	All	3.2	3.3	3.4	V
R_{FUSE}(8)	External resistor to GND for eFUSE programming (XC6SLX75, XC6SLX75T, XC6SLX100, XC6SLX100T, XC6SLX150, and XC6SLX150T only).	All	All	1129	1140	1151	Ω

Notes:
1. All voltages are relative to ground.
2. Recommended maximum voltage droop for V_{CCAUX} is 10 mV/ms.
3. Configuration data is retained even if V_{CCO} drops to 0V.
4. Includes V_{CCO} of 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V.
5. Do not exceed a total of 100 mA per bank.
6. V_{BATT} is required to maintain the battery backed RAM (BBR) AES key when V_{CCAUX} is not applied. Once V_{CCAUX} is applied, V_{BATT} can be unconnected. When BBR is not used, Xilinx recommends connecting to V_{CCAUX} or GND. However, V_{BATT} can be unconnected.
7. When programming eFUSE, $V_{FS} \leq V_{CCAUX}$. Requires up to 40 mA current. For read mode, V_{FS} can be between GND and 3.45 V.
8. R_{FUSE} is required when programming the eFUSE AES key. When not programming or when eFUSE is not used, Xilinx recommends connecting to V_{CCAUX} or GND. However, R_{FUSE} can be unconnected.

Table 3: **DC Characteristics Over Recommended Operating Conditions**

Symbol	Description	Speed Grade	Min	Typ	Max	Units
V_{DRINT}	Data retention V_{CCINT} voltage (below which configuration data might be lost)	-4, -3, -2	0.8	–	–	V
		-1L	0.8	–	–	V
V_{DRAUX}	Data retention V_{CCAUX} voltage (below which configuration data might be lost)		2.0	–	–	V
I_{REF}	V_{REF} leakage current per pin		–10	–	10	µA
I_L	Input or output leakage current per pin (sample-tested)		–10	–	10	µA
C_{IN}	Die input capacitance at the pad		–	–	10	pF
I_{RPU}	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 3.3V or V_{CCAUX} = 3.3V	-4, -3, -2	200	–	500	µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 2.5V or V_{CCAUX} = 2.5V		120	–	350	µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 1.8V		60	–	200	µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 1.5V		40	–	150	µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 1.2V		12	–	100	µA
I_{RPU}	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 3.3V or V_{CCAUX} = 3.3V	-1L				µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 2.5V or V_{CCAUX} = 2.5V					µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 1.8V					µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 1.5V					µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 1.2V					µA
I_{RPD}	Pad pull-down (when selected) @ V_{IN} = 2.5V, V_{CCAUX} = 3.3V	-4, -3, -2	200	–	550	µA
	Pad pull-down (when selected) @ V_{IN} = 2.5V, V_{CCAUX} = 2.5V		140	–	400	µA
I_{RPD}	Pad pull-down (when selected) @ V_{IN} = 2.5V, V_{CCAUX} = 3.3V	-1L				µA
	Pad pull-down (when selected) @ V_{IN} = 2.5V, V_{CCAUX} = 2.5V					µA
I_{BATT}(1)	Battery supply current		–	–	150	nA
R_{DT}(2)	Resistance of optional input differential termination circuit, V_{CCAUX} = 3.3V.			100		Ω
R_{IN_TERM}	Thevenin equivalent resistance of programmable input termination (UNTUNED_SPLIT_25)	All	23	25	55	Ω
	Thevenin equivalent resistance of programmable input termination (UNTUNED_SPLIT_50)	All	39	50	72	Ω
	Thevenin equivalent resistance of programmable input termination (UNTUNED_SPLIT_75)	All	56	75	109	Ω

Notes:
1. Maximum value specified for worst case process at 25°C. XC6SLX75, XC6SLX75T, XC6SLX100, XC6SLX100T, XC6SLX150, and XC6SLX150T only.
2. Refer to IBIS models for R_{DT} variation.
3. V_{CCO2} is not required for data retention. The minimum V_{CCO2} for power-on reset and configuration is 1.65V.

Quiescent Current (Important Note)

Typical values for quiescent supply current are specified at nominal voltage, 25°C junction temperatures (T_j). Quiescent supply current is specified by speed grade for Spartan-6 devices. Xilinx recommends analyzing static power consumption using the XPOWER™ Estimator (XPE) tool (download at http://www.xilinx.com/power) for conditions other than those specified in Table 4.

Table 4: **Typical Quiescent Supply Current**

Symbol	Description	Device	Speed Grade				Units
			-4	-3	-2	-1L	
I_{CCINTQ}	Quiescent V_{CCINT} supply current	XC6SLX4	N/A	4.0	4.0	2.4	mA
		XC6SLX9	N/A	4.0	4.0	2.4	mA
		XC6SLX16	N/A	6.0	6.0	3.6	mA
		XC6SLX25	N/A	11.0	11.0	6.6	mA
		XC6SLX25T	11.0	11.0	11.0	N/A	mA
		XC6SLX45	N/A	18.0	18.0	10.8	mA
		XC6SLX45T	18.0	18.0	18.0	N/A	mA
		XC6SLX75	N/A	30.0	30.0	18.0	mA
		XC6SLX75T	30.0	30.0	30.0	N/A	mA
		XC6SLX100	N/A	36.0	36.0	21.6	mA
		XC6SLX100T	36.0	36.0	36.0	N/A	mA
		XC6SLX150	N/A	51.0	51.0	30.6	mA
		XC6SLX150T	51.0	51.0	51.0	N/A	mA
I_{CCOQ}	Quiescent V_{CCO} supply current	XC6SLX4	N/A	1.0	1.0	1.0	mA
		XC6SLX9	N/A	1.0	1.0	1.0	mA
		XC6SLX16	N/A	2.0	2.0	2.0	mA
		XC6SLX25	N/A	2.0	2.0	2.0	mA
		XC6SLX25T	2.0	2.0	2.0	N/A	mA
		XC6SLX45	N/A	3.0	3.0	3.0	mA
		XC6SLX45T	3.0	3.0	3.0	N/A	mA
		XC6SLX75	N/A	4.0	4.0	4.0	mA
		XC6SLX75T	4.0	4.0	4.0	N/A	mA
		XC6SLX100	N/A	5.0	5.0	5.0	mA
		XC6SLX100T	5.0	5.0	5.0	N/A	mA
		XC6SLX150	N/A	7.0	7.0	7.0	mA
		XC6SLX150T	7.0	7.0	7.0	N/A	mA

Table 4: **Typical Quiescent Supply Current *(Cont'd)***

Symbol	Description	Device	Speed Grade				Units
			-4	-3	-2	-1L	
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current	XC6SLX4	N/A	3.0	3.0	3.0	mA
		XC6SLX9	N/A	3.0	3.0	3.0	mA
		XC6SLX16	N/A	3.0	3.0	3.0	mA
		XC6SLX25	N/A	4.0	4.0	4.0	mA
		XC6SLX25T	4.0	4.0	4.0	N/A	mA
		XC6SLX45	N/A	5.0	5.0	5.0	mA
		XC6SLX45T	5.0	5.0	5.0	N/A	mA
		XC6SLX75	N/A	7.0	7.0	7.0	mA
		XC6SLX75T	7.0	7.0	7.0	N/A	mA
		XC6SLX100	N/A	8.0	8.0	8.0	mA
		XC6SLX100T	8.0	8.0	8.0	N/A	mA
		XC6SLX150	N/A	12.0	12.0	12.0	mA
		XC6SLX150T	12.0	12.0	12.0	N/A	mA

Notes:
1. Typical values are specified at nominal voltage, 25°C junction temperatures (T_j). Industrial (I) grade devices have the same typical values as commercial (C) grade devices at 25°C, but higher values at 100°C. Use the XPE tool to calculate 100°C values.
2. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
3. If differential signaling is used, more accurate quiescent current estimates can be obtained by using the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools.

Table 5: **Power Supply Ramp Time**

Symbol	Description	Speed Grade	Ramp Time	Units
V_{CCINTR}	Internal supply voltage ramp time	-4, -3, -2	0.20 to 50.0	ms
		-1L	0.20 to 40.0	ms
V_{CCO2}(1)	Output drivers bank 2 supply voltage ramp time	All	0.20 to 50.0	ms
V_{CCAUXR}	Auxiliary supply voltage ramp time	All	0.20 to 50.0	ms

Notes:
1. The minimum V_{CCO2} for power-on reset and configuration is 1.65V
2. Spartan-6 FPGAs require a certain amount of supply current during power-on to insure proper device initialization. The actual current consumed depends on the power-on ramp rate of the power supply. Use the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools to estimate current drain on these supplies. Spartan-6 devices do not have a required power-on sequence.

SelectIO™ Interface DC Input and Output Levels

Table 6: **Recommended Operating Conditions for User I/Os Using Single-Ended Standards**

I/O Standard	V_{CCO} for Drivers			V_{REF} for Inputs		
	V, Min	V, Nom	V, Max	V, Min	V, Nom	V, Max
LVTTL	3.0	3.3	3.45	V_{REF} is not used for these I/O standards		
LVCMOS33	3.0	3.3	3.45			
LVCMOS25	2.3	2.5	2.7			
LVCMOS18	1.65	1.8	1.95			
LVCMOS18_JEDEC	1.65	1.8	1.95			
LVCMOS15	1.4	1.5	1.6			
LVCMOS15_JEDEC	1.4	1.5	1.6			
LVCMOS12	1.1	1.2	1.3			
LVCMOS12_JEDEC	1.1	1.2	1.3			
PCI33_3	3.0	3.3	3.45			
PCI66_3	3.0	3.3	3.45			
I2C	2.7	3.0	3.45			
SMBUS	2.7	3.0	3.45			
SDIO	3.0	3.3	3.45			
MOBILE_DDR	1.7	1.8	1.9			
HSTL_I	1.4	1.5	1.6	0.68	0.75	0.9
HSTL_II	1.4	1.5	1.6	0.68	0.75	0.9
HSTL_III	1.4	1.5	1.6	–	0.9	–
HSTL_I_18	1.7	1.8	1.9	0.8	0.9	1.1
HSTL_II_18	1.7	1.8	1.9	–	0.9	–
HSTL_III_18	1.7	1.8	1.9	–	1.1	–
SSTL3_I	3.0	3.3	3.45	1.3	1.5	1.7
SSTL3_II	3.0	3.3	3.45	1.3	1.5	1.7
SSTL2_I	2.3	2.5	2.7	1.13	1.25	1.38
SSTL2_II	2.3	2.5	2.7	1.13	1.25	1.38
SSTL18_I	1.7	1.8	1.9	0.833	0.9	0.969
SSTL18_II	1.7	1.8	1.9	0.833	0.9	0.969
SSTL15_II	1.425	1.5	1.575	0.69	0.75	0.81

Notes:

1. V_{CCO} range required when using I/O standard for an output. Also required for PCI33_3, LVCMOS18_JEDEC, LVCMOS15_JEDEC, and LVCMOS12_JEDEC inputs, and for LVCMOS25 inputs when V_{CCAUX} = 3.3V.

Table 7: **Recommended Operating Conditions for User I/Os Using Differential Signal Standards**

I/O Standard	V_{CCO} for Drivers		
	V, Min	V, Nom	V, Max
LVDS_33	3.0	3.3	3.45
LVDS_25	2.25	2.5	2.75
BLVDS_25	2.25	2.5	2.75
MINI_LVDS_33	3.0	3.3	3.45
MINI_LVDS_25	2.25	2.5	2.75
LVPECL_33 (1)	N/A–Inputs Only		
LVPECL_25	N/A–Inputs Only		
RSDS_33	3.0	3.3	3.45
RSDS_25	2.25	2.5	2.75
TMDS_33 (1)	3.14	3.3	3.45
PPDS_33	3.0	3.3	3.45
PPDS_25	2.25	2.5	2.75
DISPLAY_PORT	2.3	2.5	2.7
DIFF_HSTL_I	1.4	1.5	1.6
DIFF_HSTL_II	1.4	1.5	1.6
DIFF_HSTL_III	1.4	1.5	1.6
DIFF_HSTL_I_18	1.7	1.8	1.9
DIFF_HSTL_II_18	1.7	1.8	1.9
DIFF_HSTL_III_18	1.7	1.8	1.9
DIFF_SSTL3_I	3.0	3.3	3.45
DIFF_SSTL3_II	3.0	3.3	3.45
DIFF_SSTL2_I	2.3	2.5	2.7
DIFF_SSTL2_II	2.3	2.5	2.7
DIFF_SSTL18_I	1.7	1.8	1.9
DIFF_SSTL18_II	1.7	1.8	1.9
DIFF_SSTL15_II	1.425	1.5	1.575

Notes:

1. LVPECL_33 and TMDS_33 inputs require V_{CCAUX} = 3.3V nominal.

In Table 8 and Table 9, values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Table 8: **Single-Ended I/O Standard DC Input and Output Levels**

I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
LVTTL	–0.5	0.8	2.0	4.1	0.4	2.4	Note(2)	Note(2)
LVCMOS33	–0.5	0.8	2.0	4.1	0.4	V_{CCO} – 0.4	Note(2)	Note(2)
LVCMOS25	–0.5	0.7	1.7	4.1	0.4	V_{CCO} – 0.4	Note(2)	Note(2)
LVCMOS18	–0.5	0.38	0.8	4.1	0.45	V_{CCO} – 0.45	Note(2)	Note(2)
LVCMOS18 (-1L)	–0.5	0.33	0.71	4.1	0.45	V_{CCO} – 0.45	Note(2)	Note(2)
LVCMOS18_JEDEC	–0.5	35% V_{CCO}	65% V_{CCO}	4.1	0.45	V_{CCO} – 0.45	Note(2)	Note(2)
LVCMOS15	–0.5	0.38	0.8	4.1	25% V_{CCO}	75% V_{CCO}	Note(3)	Note(3)
LVCMOS15 (-1L)	–0.5	0.33	0.71	4.1	25% V_{CCO}	75% V_{CCO}	Note(3)	Note(3)
LVCMOS15_JEDEC	–0.5	35% V_{CCO}	65% V_{CCO}	4.1	25% V_{CCO}	75% V_{CCO}	Note(3)	Note(3)
LVCMOS12	–0.5	0.38	0.8	4.1	0.4	V_{CCO} – 0.4	Note(4)	Note(4)
LVCMOS12 (-1L)	–0.5	0.33	0.71	4.1	0.4	V_{CCO} – 0.4	Note(4)	Note(4)
LVCMOS12_JEDEC	–0.5	35% V_{CCO}	65% V_{CCO}	4.1	0.4	V_{CCO} – 0.4	Note(4)	Note(4)
PCI33_3	–0.5	30% V_{CCO}	50% V_{CCO}	V_{CCO} + 0.5	10% V_{CCO}	90% V_{CCO}	1.5	–0.5
PCI66_3	–0.5	30% V_{CCO}	50% V_{CCO}	V_{CCO} + 0.5	10% V_{CCO}	90% V_{CCO}	1.5	–0.5
I2C	–0.5	25% V_{CCO}	70% V_{CCO}	4.1	20% V_{CCO}	–	3	–
SMBUS	–0.5	0.8	2.1	4.1	0.4	–	4	–
SDIO	–0.5	12.5% V_{CCO}	75% V_{CCO}	4.1	12.5% V_{CCO}	75% V_{CCO}	0.1	–0.1
MOBILE_DDR	–0.5	20% V_{CCO}	80% V_{CCO}	4.1	10% V_{CCO}	90% V_{CCO}	0.1	–0.1
HSTL_I	–0.5	V_{REF} – 0.1	V_{REF} + 0.1	4.1	0.4	V_{CCO} – 0.4	8	–8
HSTL_II	–0.5	V_{REF} – 0.1	V_{REF} + 0.1	4.1	0.4	V_{CCO} – 0.4	16	–16
HSTL_III	–0.5	V_{REF} – 0.1	V_{REF} + 0.1	4.1	0.4	V_{CCO} – 0.4	24	–8
HSTL_I_18	–0.5	V_{REF} – 0.1	V_{REF} + 0.1	4.1	0.4	V_{CCO} – 0.4	11	–11
HSTL_II_18	–0.5	V_{REF} – 0.1	V_{REF} + 0.1	4.1	0.4	V_{CCO} – 0.4	22	–22
HSTL_III_18	–0.5	V_{REF} – 0.1	V_{REF} + 0.1	4.1	0.4	V_{CCO} – 0.4	30	–11
SSTL3_I	–0.5	V_{REF} – 0.2	V_{REF} + 0.2	4.1	V_{TT} – 0.6	V_{TT} + 0.6	8	–8
SSTL3_II	–0.5	V_{REF} – 0.2	V_{REF} + 0.2	4.1	V_{TT} – 0.8	V_{TT} + 0.8	16	–16
SSTL2_I	–0.5	V_{REF} – 0.15	V_{REF} + 0.15	4.1	V_{TT} – 0.61	V_{TT} + 0.61	8.1	–8.1
SSTL2_II	–0.5	V_{REF} – 0.15	V_{REF} + 0.15	4.1	V_{TT} – 0.81	V_{TT} + 0.81	16.2	–16.2
SSTL18_I	–0.5	V_{REF} – 0.125	V_{REF} + 0.125	4.1	V_{TT} – 0.47	V_{TT} + 0.47	6.7	–6.7
SSTL18_II	–0.5	V_{REF} – 0.125	V_{REF} + 0.125	4.1	V_{TT} – 0.60	V_{TT} + 0.60	13.4	–13.4
SSTL15_II	–0.5	V_{REF} – 0.1	V_{REF} + 0.1	4.1	V_{TT} – 0.4	V_{TT} + 0.4	13.4	–13.4

Notes:
1. Tested according to relevant specifications.
2. Using drive strengths of 2, 4, 6, 8, 12, 16, or 24 mA.
3. Using drive strengths of 2, 4, 6, 8, 12, or 16 mA.
4. Using drive strengths of 2, 4, 6, 8, or 12 mA.
5. For more information, refer to the *Spartan-6 FPGA SelectIO Resources User Guide.*

Table 9: **Differential I/O Standard DC Input and Output Levels**

I/O Standard	V_{ID}		V_{ICM}		V_{OD}		V_{OCM}		V_{OH}	V_{OL}
	mV, Min	mV, Max	V, Min	V, Max	mV, Min	mV, Max	V, Min	V, Max	V, Min	V, Max
LVDS_33	100	600	0.3	2.35	247	454	1.125	1.375	–	–
LVDS_25	100	600	0.3	2.35	247	454	1.125	1.375	–	–
BLVDS_25	100	–	0.3	2.35	240	460	Typical 50% V_{CCO}		–	–
MINI_LVDS_33	200	600	0.3	1.95	300	600	1.0	1.4	–	–
MINI_LVDS_25	200	600	0.3	1.95	300	600	1.0	1.4	–	–
LVPECL_33	100	1000	0.3	2.8(1)	Inputs only					
LVPECL_25	100	1000	0.3	1.95	Inputs only					
RSDS_33	100	–	0.3	1.5	100	400	1.0	1.4	–	–
RSDS_25	100	–	0.3	1.5	100	400	1.0	1.4	–	–
TMDS_33	150	1200	2.7	3.23(1)	400	800	V_{CCO} – 0.405	V_{CCO} – 0.190	–	–
PPDS_33	100	400	0.2	2.3	100	400	0.5	1.4	–	–
PPDS_25	100	400	0.2	2.3	100	400	0.5	1.4	–	–
DISPLAY_PORT	190	1260	0.3	2.35	–	–	Typical 50% V_{CCO}		–	–
DIFF_HSTL_I	100	–	0.68	0.9	–	–	–	–	V_{CCO} – 0.4	0.4
DIFF_HSTL_II	100	–	0.68	0.9	–	–	–	–	V_{CCO} – 0.4	0.4
DIFF_HSTL_III	100	–	0.68	0.9	–	–	–	–	V_{CCO} – 0.4	0.4
DIFF_HSTL_I_18	100	–	0.8	1.1	–	–	–	–	V_{CCO} – 0.4	0.4
DIFF_HSTL_II_18	100	–	0.8	1.1	–	–	–	–	V_{CCO} – 0.4	0.4
DIFF_HSTL_III_18	100	–	0.8	1.1	–	–	–	–	V_{CCO} – 0.4	0.4
DIFF_SSTL3_I	100	–	1.0	1.9	–	–	–	–	V_{TT} + 0.6	V_{TT} – 0.6
DIFF_SSTL3_II	100	–	1.0	1.9	–	–	–	–	V_{TT} + 0.8	V_{TT} – 0.8
DIFF_SSTL2_I	100	–	1.0	1.5	–	–	–	–	V_{TT} + 0.61	V_{TT} – 0.61
DIFF_SSTL2_II	100	–	1.0	1.5	–	–	–	–	V_{TT} + 0.81	V_{TT} – 0.81
DIFF_SSTL18_I	100	–	0.7	1.1	–	–	–	–	V_{TT} + 0.47	V_{TT} – 0.47
DIFF_SSTL18_II	100	–	0.7	1.1	–	–	–	–	V_{TT} + 0.6	V_{TT} – 0.6
DIFF_SSTL15_II	100	–	0.55	0.95	–	–	–	–	V_{TT} + 0.4	V_{TT} – 0.4

Notes:

1. LVPECL_33 and TMDS_33 maximum V_{ICM} is the lower of V (maximum) or V_{CCAUX} – (V_{ID}/2)

eFUSE Read Endurance

Table 10 lists the minimum guaranteed number of read cycle operations for Device DNA and for the AES eFUSE key. For more information, see the *Spartan-6 FPGA Configuration User Guide*.

Table 10: **eFUSE Read Endurance**

Symbol	Description	Speed Grade				Units (Min)
		-4	-3	-2	-1L	
DNA_CYCLES	Number of DNA_PORT READ operations or JTAG ISC_DNA read command operations. Unaffected by SHIFT operations.	30,000,000				Read Cycles
AES_CYCLES	Number of JTAG FUSE_KEY or FUSE_CNTL read command operations. Unaffected by SHIFT operations.	30,000,000				Read Cycles

GTP Transceiver Specifications

GTP transceivers are available in the Spartan-6 LXT family of devices. See DS160: *Spartan-6 Family Overview* for more information.

GTP Transceiver DC Characteristics

Table 11: **Absolute Maximum Ratings for GTP Transceivers(1)**

Symbol	Description	Mln	Max	Units
MGTAVCC	Analog supply voltage for the GTP transmitter and receiver circuits relative to GND	–0.5	1.32	V
MGTAVTTTX	Analog supply voltage for the GTP transmitter termination circuit relative to GND	–0.5	1.32	V
MGTAVTTRX	Analog supply voltage for the GTP receiver termination circuit relative to GND	–0.5	1.32	V
MGTAVCCPLL	Analog supply voltage for the GTP transmitter and receiver PLL circuits relative to GND	–0.5	1.32	V
MGTAVTTRCAL	Analog supply voltage for the resistor calibration circuit of the GTP transceiver bank (top or bottom)	–0.5	1.32	V
V_{IN}	Receiver (RXP/RXN) and Transmitter (TXP/TXN) absolute input voltage	–0.5	1.32	V
$V_{MGTREFCLK}$	Reference clock absolute input voltage	–0.5	1.32	V

Notes:
1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.

Table 12: **Recommended Operating Conditions for GTP Transceivers(1,2)**

Symbol	Description	Min	Typ	Max	Units
MGTAVCC	Analog supply voltage for the GTP transmitter and receiver circuits relative to GND	1.14	1.20	1.26	V
MGTAVTTTX	Analog supply voltage for the GTP transmitter termination circuit relative to GND	1.14	1.20	1.26	V
MGTAVTTRX	Analog supply voltage for the GTP receiver termination circuit relative to GND	1.14	1.20	1.26	V
MGTAVCCPLL	Analog supply voltage for the GTP transmitter and receiver PLL circuits relative to GND	1.14	1.20	1.26	V
MGTAVTTRCAL	Analog supply voltage for the resistor calibration circuit of the GTP transceiver bank (top or bottom)	1.14	1.20	1.26	V

Notes:
1. Each voltage listed requires the filter circuit described in *Spartan-6 FPGA GTP Transceivers User Guide*.
2. Voltages are specified for the temperature range of T_j = –40°C to +100°C.

Table 13: **GTP Transceiver Current Supply (per Lane)**

Symbol	Description	Typ(1)	Max	Units
$I_{MGTAVCC}$	GTP transceiver internal analog supply current	40.4	Note 2	mA
$I_{MGTAVTTTX}$	GTP transmitter termination supply current	27.4		mA
$I_{MGTAVTTRX}$	GTP receiver termination supply current	13.6		mA
$I_{MGTAVCCPLL}$	GTP transmitter and receiver PLL supply current	28.7		mA
$R_{MGTRREF}$	Precision reference resistor for internal calibration termination	50.0 ± 1% tolerance		Ω

Notes:
1. Typical values are specified at nominal voltage, 25°C, with a 2.5 Gb/s line rate, with a shared PLL use mode.
2. Values for currents of other transceiver configurations and conditions can be obtained by using the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools.

Table 14: **GTP Transceiver Quiescent Supply Current (per Lane)(1,2,3)**

Symbol	Description	Typ(4)	Max	Units
$I_{MGTAVCCQ}$	Quiescent MGTAVCC supply current	1.7	Note 2	mA
$I_{MGTAVTTTXQ}$	Quiescent MGTAVTTTX supply current	0.1		mA
$I_{MGTAVTTRXQ}$	Quiescent MGTAVTTRX supply current	1.2		mA
$I_{MGTAVCCPLLQ}$	Quiescent MGTAVCCPLL supply current	1.0		mA

Notes:
1. Device powered and unconfigured.
2. Currents for conditions other than values specified in this table can be obtained by using the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools.
3. GTP transceiver quiescent supply current for an entire device can be calculated by multiplying the values in this table by the number of available GTP transceivers.
4. Typical values are specified at nominal voltage, 25°C.

GTP Transceiver DC Input and Output Levels

Table 15 summarizes the DC output specifications of the GTP transceivers in Spartan-6 FPGAs. Figure 1 shows the single-ended output voltage swing. Figure 2 shows the peak-to-peak differential output voltage.

Consult UG386: *Spartan-6 FPGA GTP Transceivers User Guide* for further details.

Table 15: **GTP Transceiver DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
DV_{PPIN}	Differential peak-to-peak input voltage	External AC coupled	125		2000	mV
V_{IN}	Absolute input voltage	DC coupled MGTAVTTRX = 1.2V	–400		MGTAVTTRX	mV
V_{CMIN}	Common mode input voltage	DC coupled MGTAVTTRX = 1.2V		3/4 MGTAVTTRX		mV
DV_{PPOUT}	Differential peak-to-peak output voltage(1)	Transmitter output swing is set to maximum setting			1000	mV
V_{SEOUT}	Single-ended output voltage swing(1)				500	mV
$V_{CMOUTDC}$	Common mode output voltage	Equation based	MGTAVTTTX – V_{SEOUT}/2			mV
R_{IN}	Differential input resistance		80	100	130	Ω
R_{OUT}	Differential output resistance		80	100	130	Ω
T_{OSKEW}	Transmitter output skew				15	ps
C_{EXT}	Recommended external AC coupling capacitor(2)		75	100	200	nF

Notes:
1. The output swing and preemphasis levels are programmable using the attributes discussed in the *Spartan-6 FPGA GTP Transceivers User Guide* and can result in values lower than reported in this table.
2. Other values can be used as appropriate to conform to specific protocols and standards.

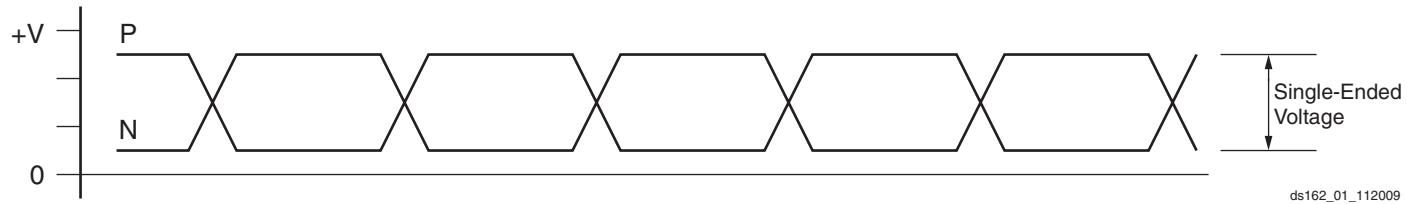

Figure 1: **Single-Ended Peak-to-Peak Voltage**

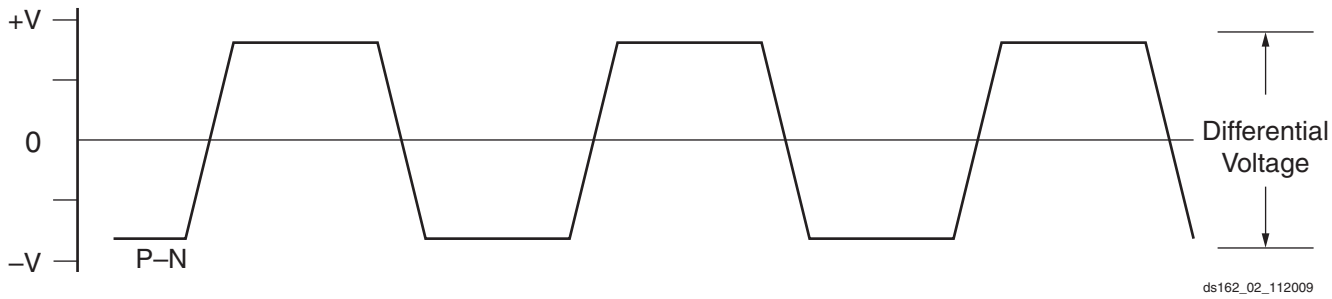

Figure 2: **Differential Peak-to-Peak Voltage**

Table 16 summarizes the DC specifications of the clock input of the GTP transceiver. Consult the *Spartan-6 FPGA GTP Transceivers User Guide* for further details.

Table 16: **GTP Transceiver Clock DC Input Level Specification(1)**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{IDIFF}	Differential peak-to-peak input voltage		200	800	2000	mV
R_{IN}	Differential input resistance		80	100	120	Ω
C_{EXT}	Required external AC coupling capacitor			100		nF

GTP Transceiver Switching Characteristics

Consult the *Spartan-6 FPGA GTP Transceivers User Guide* for further information.

Table 17: **GTP Transceiver Performance**

Symbol	Description	Speed Grade				Units
		-4	-3	-2	-1L	
F_{GTPMAX}	Maximum GTP transceiver data rate	3.125	3.125	2.7	N/A	Gb/s
$F_{GTPRANGE1}$	GTP transceiver data rate range when PLL_TXDIVSEL_OUT = 1	2.4 to 3.125	2.4 to 3.125	2.4 to 2.7	N/A	Gb/s
$F_{GTPRANGE2}$	GTP transceiver data rate range when PLL_TXDIVSEL_OUT = 2	1.2 to 1.62	1.2 to 1.62	1.2 to 1.62	N/A	Gb/s
$F_{GTPRANGE3}$	GTP transceiver data rate range when PLL_TXDIVSEL_OUT = 4	0.6 to 0.81	0.6 to 0.81	0.6 to 0.81	N/A	Gb/s
$F_{GPLLMAX}$	Maximum PLL frequency	1.62	1.62	1.62	N/A	GHz
$F_{GPLLMIN}$	Minimum PLL frequency	1.2	1.2	1.2	N/A	GHz

Table 18: **GTP Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-4	-3	-2	-1L	
$F_{GTPDRPCLK}$	GTP transceiver DCLK (DRP clock) maximum frequency	160	156.25	100	N/A	MHz

Table 19: **GTP Transceiver Reference Clock Switching Characteristics**

Symbol	Description	Conditions	All LXT Speed Grades			Units
			Min	Typ	Max	
F_{GCLK}	Reference clock frequency range		60		160	MHz
T_{RCLK}	Reference clock rise time	20% – 80%		200		ps
T_{FCLK}	Reference clock fall time	80% – 20%		200		ps
T_{DCREF}	Reference clock duty cycle	Transceiver PLL only	45	50	55	%
T_{LOCK}	Clock recovery frequency acquisition time	Initial PLL lock			1	ms
T_{PHASE}	Clock recovery phase acquisition time	Lock to data after PLL has locked to the reference clock			200	µs

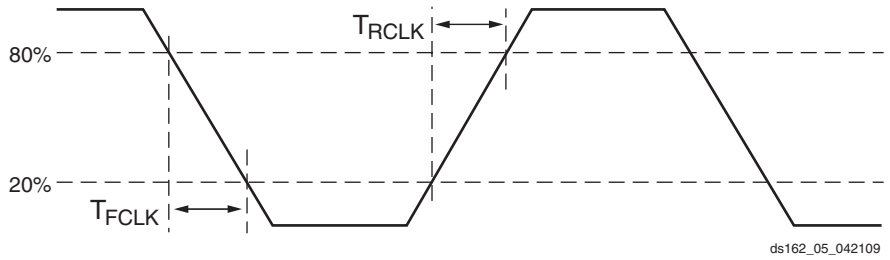

Figure 3: **Reference Clock Timing Parameters**

Table 20: **GTP Transceiver User Clock Switching Characteristics(1)**

Symbol	Description	Conditions	Speed Grade				Units
			-4	-3	-2	-1L	
F_{TXOUT}	TXOUTCLK maximum frequency		312.5	312.5	270	N/A	MHz
F_{RXREC}	RXRECCLK maximum frequency		312.5	312.5	270	N/A	MHz
T_{RX}	RXUSRCLK maximum frequency		312.5	312.5	270	N/A	MHz
T_{RX2}	RXUSRCLK2 maximum frequency	1 byte interface	156.25	156.25	125	N/A	MHz
		2 byte interface	156.25	156.25	125	N/A	MHz
		4 byte interface	78.125	78.125	67.5	N/A	MHz
T_{TX}	TXUSRCLK maximum frequency		312.5	312.5	270	N/A	MHz
T_{TX2}	TXUSRCLK2 maximum frequency	1 byte interface	156.25	156.25	125	N/A	MHz
		2 byte interface	156.25	156.25	125	N/A	MHz
		4 byte interface	78.125	78.125	67.5	N/A	MHz

Notes:
1. Clocking must be implemented as described in the *Spartan-6 FPGA GTP Transceivers User Guide*.

Table 21: **GTP Transceiver Transmitter Switching Characteristics**

Symbol	Description	Condition	Min	Typ	Max	Units
T_{RTX}	TX Rise time	20%–80%		140		ps
T_{FTX}	TX Fall time	80%–20%		120		ps
T_{LLSKEW}	TX lane-to-lane skew(1)				200	ps
$V_{TXOOBVDPP}$	Electrical idle amplitude				20	mV
$T_{TXOOBTRANSITION}$	Electrical idle transition time				50	ns
$T_{J3.125}$	Total Jitter(2)	3.125 Gb/s			0.35	UI
$D_{J3.125}$	Deterministic Jitter(2)				0.15	UI
$T_{J2.5}$	Total Jitter(2)	2.5 Gb/s			0.33	UI
$D_{J2.5}$	Deterministic Jitter(2)				0.15	UI
$T_{J1.62}$	Total Jitter(2)	1.62 Gb/s			0.20	UI
$D_{J1.62}$	Deterministic Jitter(2)				0.10	UI
$T_{J1.25}$	Total Jitter(2)	1.25 Gb/s			0.20	UI
$D_{J1.25}$	Deterministic Jitter(2)				0.10	UI
T_{J614}	Total Jitter(2)	614 Mb/s			0.10	UI
D_{J614}	Deterministic Jitter(2)				0.05	UI

Notes:
1. Using same REFCLK input with TXENPMAPHASEALIGN enabled for up to four consecutive GTP transceiver sites.
2. Using PLL_DIVSEL_FB = 2, INTDATAWIDTH = 1. These values are NOT intended for protocol specific compliance determinations.

Table 22: **GTP Transceiver Receiver Switching Characteristics**

Symbol	Description		Min	Typ	Max	Units
$T_{RXELECIDLE}$	Time for RXELECIDLE to respond to loss or restoration of data			75		ns
$R_{XOOBVDPP}$	OOB detect threshold peak-to-peak		60		150	mV
R_{XSST}	Receiver spread-spectrum tracking(1)	Modulated @ 33 KHz	–5000		0	ppm
R_{XRL}	Run length (CID)	Internal AC capacitor bypassed			150	UI
$R_{XPPMTOL}$	Data/REFCLK PPM offset tolerance	CDR 2nd-order loop disabled	–200		200	ppm
		CDR 2nd-order loop enabled	–2000		2000	ppm
SJ Jitter Tolerance(2)						
$JT\_SJ_{3.125}$	Sinusoidal Jitter(3)	3.125 Gb/s	0.4			UI
$JT\_SJ_{2.5}$	Sinusoidal Jitter(3)	2.5 Gb/s	0.4			UI
$JT\_SJ_{1.62}$	Sinusoidal Jitter(3)	1.62 Gb/s	0.5			UI
$JT\_SJ_{1.25}$	Sinusoidal Jitter(3)	1.25 Gb/s	0.5			UI
JT_SJ_{614}	Sinusoidal Jitter(3)	614 Mb/s	0.5			UI
SJ Jitter Tolerance with Stressed Eye(2)						
$JT\_TJSE_{3.125}$	Total Jitter with Stressed Eye	3.125 Gb/s				UI
$JT\_SJSE_{3.125}$	Sinusoidal Jitter with Stressed Eye	3.125 Gb/s				UI

Notes:
1. Using PLL_RXDIVSEL_OUT = 1, 2, and 4.
2. All jitter values are based on a Bit Error Ratio of $1e^{-12}$.
3. Using 80 MHz sinusoidal jitter only in the absence of deterministic and random jitter.

Endpoint Block for PCI Express Designs Switching Characteristics

The Endpoint block for PCI Express is available in the Spartan-6 LXT family. Consult the Spartan-6 FPGA Integrated Endpoint Block for PCI Express for further information.

Table 23: **Maximum Performance for PCI Express Designs**

Symbol	Description	Speed Grade				Units
		-4	-3	-2	-1L	
$F_{PCIEUSER}$	User clock maximum frequency	62.5	62.5	62.5	N/A	MHz

Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Spartan-6 devices. The numbers reported here are worst-case values; they have all been fully characterized. These values are subject to the same guidelines as the Switching Characteristics, page 16.

Table 24: **Interface Performances**

Description	Speed Grade				Units
	-4	-3	-2	-1L	
Networking Applications (1)					
SDR LVDS transmitter or receiver (using IOB SDR register)	400	400	375		Mb/s
DDR LVDS transmitter or receiver (using IOB ODDR2/IDDR2 register)	800	800	750		Mb/s
SDR LVDS transmitter (using OSERDES2; DATA WIDTH = 2 to 8)	1050	1050	950		Mb/s
DDR LVDS transmitter (using OSERDES2; DATA WIDTH = 2 to 8)	1050	1050	950		Mb/s
Memory Interfaces (Implemented using the Spartan-6 FPGA Memory Controller Block) (2)					
DDR	400	400	400		Mb/s
DDR2	800	800	667		Mb/s
DDR3	800	800	667		Mb/s
LPDDR (Mobile_DDR)	400	400	400		Mb/s

Notes:
1. LVDS receivers are typically bounded with certain applications where specific DPA algorithms dominate deterministic performance.
2. Refer to XAPP1064, *Source-Synchronous Serialization and Deserialization (up to 1050 Mb/s).*
3. Refer to the *Spartan-6 FPGA Memory Controller User Guide*

Switching Characteristics

All values represented in this data sheet are based on these speed specifications: v1.07 for -4, -3, and -2; and v1.00 for -1L. Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

Advance

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Production

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

All specifications are always representative of worst-case supply voltage and junction temperature conditions.

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device.

Table 25 correlates the current status of each Spartan-6 device on a per speed grade basis.

Table 25: **Spartan-6 Device Speed Grade Designations**

Device	Speed Grade Designations		
	Advance	Preliminary	Production
XC6SLX4	-3, -2, -1L		
XC6SLX9	-3, -2, -1L		
XC6SLX16	-3, -1L		-2
XC6SLX25	-3, -2, -1L		
XC6SLX25T	-4, -3, -2		
XC6SLX45	-3, -1L		-2
XC6SLX45T	-4, -3, -2		
XC6SLX75	-3, -2, -1L		
XC6SLX75T	-4, -3, -2		
XC6SLX100	-3, -2, -1L		
XC6SLX100T	-4, -3, -2		
XC6SLX150	-3, -2, -1L		
XC6SLX150T	-4, -3, -2		

Testing of Switching Characteristics

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Spartan-6 devices.

Production Silicon and ISE Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label (Advance, Preliminary, Production). Any labeling discrepancies are corrected in subsequent speed specification releases. Table 26 lists the production released Spartan-6 family member, speed grade, and the minimum corresponding supported speed specification version and ISE® software revisions. The ISE software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

Table 26: **Spartan-6 Device Production Software and Speed Specification Release(1)**

Device	Speed Grade Designations(2)			
	-4	-3	-2	-1L
XC6SLX4	N/A			
XC6SLX9	N/A			
XC6SLX16	N/A		ISE 11.5 v1.06	
XC6SLX25	N/A			
XC6SLX25T				N/A
XC6SLX45	N/A		ISE 11.5 v1.07	
XC6SLX45T				N/A
XC6SLX75	N/A			
XC6SLX75T				N/A
XC6SLX100	N/A			
XC6SLX100T				N/A
XC6SLX150	N/A			
XC6SLX150T				N/A

Notes:
1. Blank entries indicate a device and/or speed grade in advance or preliminary status.
2. LX devices are not available with a -4 speed grade; LXT devices are not available with a -1L speed grade.

IOB Pad Input/Output/3-State Switching Characteristics

Table 27 summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard) and 3-state delays.

T_{IOPI} is described as the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.

T_{IOOP} is described as the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.

T_{IOTP} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer.

Table 28 summarizes the value of T_{IOTPHZ}. T_{IOTPHZ} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state).

Table 27: **IOB Switching Characteristics**

I/O Standard	T_{IOPI}				T_{IOOP}				T_{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-4	-3	-2	-1L	-4	-3	-2	-1L	-4	-3	-2	-1L	
LVDS_33	1.28	1.29	1.42	1.80	1.60	1.69	1.89	2.28	1.60	1.69	1.89	2.28	ns
LVDS_25	1.12	1.13	1.26	1.63	1.70	1.79	1.99	2.44	1.70	1.79	1.99	2.44	ns
BLVDS_25	1.13	1.14	1.27	1.63	1.77	1.86	2.06	2.62	1.77	1.86	2.06	2.62	ns
MINI_LVDS_33	1.28	1.29	1.42	1.80	1.62	1.71	1.91	2.27	1.62	1.71	1.91	2.27	ns
MINI_LVDS_25	1.12	1.13	1.26	1.63	1.70	1.79	1.99	2.44	1.70	1.79	1.99	2.44	ns

Table 27: **IOB Switching Characteristics *(Cont'd)***

I/O Standard	T_{IOPI}				T_{IOOP}				T_{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-4	-3	-2	-1L	-4	-3	-2	-1L	-4	-3	-2	-1L	
LVPECL_33	1.29	1.30	1.43	1.80	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	ns
LVPECL_25	1.13	1.14	1.27	1.63	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	ns
RSDS_33 (point to point)	1.28	1.29	1.42	1.80	1.62	1.71	1.91	2.28	1.62	1.71	1.91	2.28	ns
RSDS_25 (point to point)	1.12	1.13	1.26	1.63	1.70	1.79	1.99	2.43	1.70	1.79	1.99	2.43	ns
TMDS_33	1.32	1.33	1.46	1.83	1.59	1.68	1.88	2.22	1.59	1.68	1.88	2.22	ns
PPDS_33	1.28	1.29	1.42	1.80	1.62	1.71	1.91	2.28	1.62	1.71	1.91	2.28	ns
PPDS_25	1.12	1.13	1.26	1.63	1.73	1.82	2.02	2.44	1.73	1.82	2.02	2.44	ns
PCI33_3	1.18	1.19	1.32		3.56	3.65	3.85		3.56	3.65	3.85		ns
PCI66_3	1.18	1.19	1.32		3.56	3.65	3.85		3.56	3.65	3.85		ns
DISPLAY_PORT	1.13	1.14	1.27	1.63	3.20	3.29	3.49	3.99	3.20	3.29	3.49	3.99	ns
I2C	1.44	1.45	1.58	1.99	11.61	11.70	11.90	7.67	11.61	11.70	11.90	7.67	ns
SMBUS	1.44	1.45	1.58	1.99	11.61	11.70	11.90	7.67	11.61	11.70	11.90	7.67	ns
SDIO	1.47	1.48	1.61	2.02	2.69	2.78	2.98	3.64	2.69	2.78	2.98	3.64	ns
MOBILE_DDR	1.05	1.06	1.19	1.51	2.40	2.49	2.69	3.40	2.40	2.49	2.69	3.40	ns
HSTL_I	1.01	1.02	1.15	1.46	1.71	1.80	2.00	2.39	1.71	1.80	2.00	2.39	ns
HSTL_II	1.02	1.03	1.16	1.46	1.77	1.86	2.06	2.38	1.77	1.86	2.06	2.38	ns
HSTL_III	1.06	1.07	1.20	1.53	1.72	1.81	2.01	2.42	1.72	1.81	2.01	2.42	ns
HSTL_I _18	1.05	1.06	1.19	1.52	1.82	1.91	2.11	2.43	1.82	1.91	2.11	2.43	ns
HSTL_II _18	1.05	1.06	1.19	1.52	1.90	1.99	2.19	2.46	1.90	1.99	2.19	2.46	ns
HSTL_III _18	1.10	1.11	1.24	1.58	1.84	1.93	2.13	2.33	1.84	1.93	2.13	2.33	ns
SSTL3_I	1.69	1.70	1.83	2.30	1.88	1.97	2.17	2.38	1.88	1.97	2.17	2.38	ns
SSTL3_II	1.69	1.70	1.83	2.30	2.06	2.15	2.35	2.43	2.06	2.15	2.35	2.43	ns
SSTL2_I	1.41	1.42	1.55	1.95	1.82	1.91	2.11	2.33	1.82	1.91	2.11	2.33	ns
SSTL2_II	1.41	1.42	1.55	1.96	1.91	2.00	2.20	2.39	1.91	2.00	2.20	2.39	ns
SSTL18_I	1.03	1.04	1.17	1.47	1.68	1.77	1.97	2.27	1.68	1.77	1.97	2.27	ns
SSTL18_II	1.03	1.04	1.17	1.46	1.71	1.80	2.00	2.31	1.71	1.80	2.00	2.31	ns
SSTL15_II	1.03	1.04	1.17	1.44	1.72	1.81	2.01	2.34	1.72	1.81	2.01	2.34	ns
DIFF_HSTL_I	1.05	1.06	1.19	1.52	1.82	1.91	2.11	2.44	1.82	1.91	2.11	2.44	ns
DIFF_HSTL_II	1.04	1.05	1.18	1.52	1.77	1.86	2.06	2.39	1.77	1.86	2.06	2.39	ns
DIFF_HSTL_III	1.04	1.05	1.18	1.52	1.74	1.83	2.03	2.37	1.74	1.83	2.03	2.37	ns
DIFF_HSTL_I_18	1.08	1.09	1.22	1.57	1.84	1.93	2.13	2.46	1.84	1.93	2.13	2.46	ns
DIFF_HSTL_II_18	1.08	1.09	1.22	1.56	1.74	1.83	2.03	2.37	1.74	1.83	2.03	2.37	ns
DIFF_HSTL_III_18	1.08	1.09	1.22	1.57	1.74	1.83	2.03	2.39	1.74	1.83	2.03	2.39	ns
DIFF_SSTL3_I	1.29	1.30	1.43	1.80	1.86	1.95	2.15	2.44	1.86	1.95	2.15	2.44	ns
DIFF_SSTL3_II	1.30	1.31	1.44	1.80	1.85	1.94	2.14	2.48	1.85	1.94	2.14	2.48	ns
DIFF_SSTL2_I	1.13	1.14	1.27	1.63	1.85	1.94	2.14	2.46	1.85	1.94	2.14	2.46	ns
DIFF_SSTL2_II	1.13	1.14	1.27	1.63	1.81	1.90	2.10	2.44	1.81	1.90	2.10	2.44	ns
DIFF_SSTL18_I	1.08	1.09	1.22	1.57	1.77	1.86	2.06	2.37	1.77	1.86	2.06	2.37	ns

Table 27: **IOB Switching Characteristics *(Cont'd)***

I/O Standard	T_{IOPI}				T_{IOOP}				T_{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-4	-3	-2	-1L	-4	-3	-2	-1L	-4	-3	-2	-1L	
DIFF_SSTL18_II	1.09	1.10	1.23	1.57	1.73	1.82	2.02	2.37	1.73	1.82	2.02	2.37	ns
DIFF_SSTL15_II	1.05	1.06	1.19	1.53	1.72	1.81	2.01	2.34	1.72	1.81	2.01	2.34	ns
LVTTL, QUIETIO, 2 mA	1.46	1.47	1.60	2.02	5.44	5.53	5.73	6.82	5.44	5.53	5.73	6.82	ns
LVTTL, QUIETIO, 4 mA	1.46	1.47	1.60	2.02	4.34	4.43	4.63	5.46	4.34	4.43	4.63	5.46	ns
LVTTL, QUIETIO, 6 mA	1.46	1.47	1.60	2.02	3.80	3.89	4.09	4.89	3.80	3.89	4.09	4.89	ns
LVTTL, QUIETIO, 8 mA	1.46	1.47	1.60	2.02	3.28	3.37	3.57	4.31	3.28	3.37	3.57	4.31	ns
LVTTL, QUIETIO, 12 mA	1.46	1.47	1.60	2.02	3.33	3.42	3.62	4.32	3.33	3.42	3.62	4.32	ns
LVTTL, QUIETIO, 16 mA	1.46	1.47	1.60	2.02	2.99	3.08	3.28	3.98	2.99	3.08	3.28	3.98	ns
LVTTL, QUIETIO, 24 mA	1.46	1.47	1.60	2.02	2.74	2.83	3.03	3.72	2.74	2.83	3.03	3.72	ns
LVTTL, Slow, 2 mA	1.46	1.47	1.60	2.02	4.41	4.50	4.70	5.68	4.41	4.50	4.70	5.68	ns
LVTTL, Slow, 4 mA	1.46	1.47	1.60	2.02	3.22	3.31	3.51	4.29	3.22	3.31	3.51	4.29	ns
LVTTL, Slow, 6 mA	1.46	1.47	1.60	2.02	2.81	2.90	3.10	3.82	2.81	2.90	3.10	3.82	ns
LVTTL, Slow, 8 mA	1.46	1.47	1.60	2.02	2.64	2.73	2.93	3.64	2.64	2.73	2.93	3.64	ns
LVTTL, Slow, 12 mA	1.46	1.47	1.60	2.02	2.63	2.72	2.92	3.53	2.63	2.72	2.92	3.53	ns
LVTTL, Slow, 16 mA	1.46	1.47	1.60	2.02	2.44	2.53	2.73	3.38	2.44	2.53	2.73	3.38	ns
LVTTL, Slow, 24 mA	1.46	1.47	1.60	2.02	2.33	2.42	2.62	3.04	2.33	2.42	2.62	3.04	ns
LVTTL, Fast, 2 mA	1.46	1.47	1.60	2.02	3.83	3.92	4.12	5.00	3.83	3.92	4.12	5.00	ns
LVTTL, Fast, 4 mA	1.46	1.47	1.60	2.02	2.54	2.63	2.83	3.57	2.54	2.63	2.83	3.57	ns
LVTTL, Fast, 6 mA	1.46	1.47	1.60	2.02	2.49	2.58	2.78	3.12	2.49	2.58	2.78	3.12	ns
LVTTL, Fast, 8 mA	1.46	1.47	1.60	2.02	2.37	2.46	2.66	2.91	2.37	2.46	2.66	2.91	ns
LVTTL, Fast, 12 mA	1.46	1.47	1.60	2.02	1.88	1.97	2.17	2.75	1.88	1.97	2.17	2.75	ns
LVTTL, Fast, 16 mA	1.46	1.47	1.60	2.02	1.88	1.97	2.17	2.70	1.88	1.97	2.17	2.70	ns
LVTTL, Fast, 24 mA	1.46	1.47	1.60	2.02	1.88	1.97	2.17	2.70	1.88	1.97	2.17	2.70	ns
LVCMOS33, QUIETIO, 2 mA	1.45	1.46	1.59	2.02	5.45	5.54	5.74	6.82	5.45	5.54	5.74	6.82	ns
LVCMOS33, QUIETIO, 4 mA	1.45	1.46	1.59	2.02	4.08	4.17	4.37	5.28	4.08	4.17	4.37	5.28	ns
LVCMOS33, QUIETIO, 6 mA	1.45	1.46	1.59	2.02	3.56	3.65	3.85	4.67	3.56	3.65	3.85	4.67	ns
LVCMOS33, QUIETIO, 8 mA	1.45	1.46	1.59	2.02	3.42	3.51	3.71	4.43	3.42	3.51	3.71	4.43	ns
LVCMOS33, QUIETIO, 12 mA	1.45	1.46	1.59	2.02	2.99	3.08	3.28	3.96	2.99	3.08	3.28	3.96	ns
LVCMOS33, QUIETIO, 16 mA	1.45	1.46	1.59	2.02	2.82	2.91	3.11	3.81	2.82	2.91	3.11	3.81	ns
LVCMOS33, QUIETIO, 24 mA	1.45	1.46	1.59	2.02	2.64	2.73	2.93	3.64	2.64	2.73	2.93	3.64	ns
LVCMOS33, Slow, 2 mA	1.45	1.46	1.59	2.02	4.42	4.51	4.71	5.68	4.42	4.51	4.71	5.68	ns
LVCMOS33, Slow, 4 mA	1.45	1.46	1.59	2.02	3.03	3.12	3.32	4.10	3.03	3.12	3.32	4.10	ns
LVCMOS33, Slow, 6 mA	1.45	1.46	1.59	2.02	2.63	2.72	2.92	3.63	2.63	2.72	2.92	3.63	ns
LVCMOS33, Slow, 8 mA	1.45	1.46	1.59	2.02	2.70	2.79	2.99	3.64	2.70	2.79	2.99	3.64	ns
LVCMOS33, Slow, 12 mA	1.45	1.46	1.59	2.02	2.44	2.53	2.73	3.33	2.44	2.53	2.73	3.33	ns
LVCMOS33, Slow, 16 mA	1.45	1.46	1.59	2.02	2.36	2.45	2.65	3.33	2.36	2.45	2.65	3.33	ns
LVCMOS33, Slow, 24 mA	1.45	1.46	1.59	2.02	2.33	2.42	2.62	3.03	2.33	2.42	2.62	3.03	ns
LVCMOS33, Fast, 2 mA	1.45	1.46	1.59	2.02	3.81	3.90	4.10	5.02	3.81	3.90	4.10	5.02	ns

Table 27: **IOB Switching Characteristics *(Cont'd)***

I/O Standard	T_{IOPI}				T_{IOOP}				T_{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-4	-3	-2	-1L	-4	-3	-2	-1L	-4	-3	-2	-1L	
LVCMOS33, Fast, 4 mA	1.45	1.46	1.59	2.02	2.53	2.62	2.82	3.58	2.53	2.62	2.82	3.58	ns
LVCMOS33, Fast, 6 mA	1.45	1.46	1.59	2.02	2.37	2.46	2.66	3.12	2.37	2.46	2.66	3.12	ns
LVCMOS33, Fast, 8 mA	1.45	1.46	1.59	2.02	2.12	2.21	2.41	2.88	2.12	2.21	2.41	2.88	ns
LVCMOS33, Fast, 12 mA	1.45	1.46	1.59	2.02	1.70	1.79	1.99	2.61	1.70	1.79	1.99	2.61	ns
LVCMOS33, Fast, 16 mA	1.45	1.46	1.59	2.02	1.70	1.79	1.99	2.61	1.70	1.79	1.99	2.61	ns
LVCMOS33, Fast, 24 mA	1.45	1.46	1.59	2.02	1.70	1.79	1.99	2.61	1.70	1.79	1.99	2.61	ns
LVCMOS25, QUIETIO, 2 mA	0.93	0.94	1.07	1.41	4.86	4.95	5.15	6.18	4.86	4.95	5.15	6.18	ns
LVCMOS25, QUIETIO, 4 mA	0.93	0.94	1.07	1.41	3.75	3.84	4.04	4.89	3.75	3.84	4.04	4.89	ns
LVCMOS25, QUIETIO, 6 mA	0.93	0.94	1.07	1.41	3.51	3.60	3.80	4.53	3.51	3.60	3.80	4.53	ns
LVCMOS25, QUIETIO, 8 mA	0.93	0.94	1.07	1.41	3.25	3.34	3.54	4.24	3.25	3.34	3.54	4.24	ns
LVCMOS25, QUIETIO, 12 mA	0.93	0.94	1.07	1.41	2.88	2.97	3.17	3.86	2.88	2.97	3.17	3.86	ns
LVCMOS25, QUIETIO, 16 mA	0.93	0.94	1.07	1.41	2.69	2.78	2.98	3.65	2.69	2.78	2.98	3.65	ns
LVCMOS25, QUIETIO, 24 mA	0.93	0.94	1.07	1.41	2.50	2.59	2.79	3.47	2.50	2.59	2.79	3.47	ns
LVCMOS25, Slow, 2 mA	0.93	0.94	1.07	1.41	3.83	3.92	4.12	5.01	3.83	3.92	4.12	5.01	ns
LVCMOS25, Slow, 4 mA	0.93	0.94	1.07	1.41	2.84	2.93	3.13	3.87	2.84	2.93	3.13	3.87	ns
LVCMOS25, Slow, 6 mA	0.93	0.94	1.07	1.41	2.78	2.87	3.07	3.77	2.78	2.87	3.07	3.77	ns
LVCMOS25, Slow, 8 mA	0.93	0.94	1.07	1.41	2.53	2.62	2.82	3.50	2.53	2.62	2.82	3.50	ns
LVCMOS25, Slow, 12 mA	0.93	0.94	1.07	1.41	2.06	2.15	2.35	2.99	2.06	2.15	2.35	2.99	ns
LVCMOS25, Slow, 16 mA	0.93	0.94	1.07	1.41	2.06	2.15	2.35	2.99	2.06	2.15	2.35	2.99	ns
LVCMOS25, Slow, 24 mA	0.93	0.94	1.07	1.41	2.06	2.15	2.35	2.75	2.06	2.15	2.35	2.75	ns
LVCMOS25, Fast, 2 mA	0.93	0.94	1.07	1.41	3.40	3.49	3.69	4.52	3.40	3.49	3.69	4.52	ns
LVCMOS25, Fast, 4 mA	0.93	0.94	1.07	1.41	2.30	2.39	2.59	3.30	2.30	2.39	2.59	3.30	ns
LVCMOS25, Fast, 6 mA	0.93	0.94	1.07	1.41	2.14	2.23	2.43	2.82	2.14	2.23	2.43	2.82	ns
LVCMOS25, Fast, 8 mA	0.93	0.94	1.07	1.41	2.07	2.16	2.36	2.74	2.07	2.16	2.36	2.74	ns
LVCMOS25, Fast, 12 mA	0.93	0.94	1.07	1.41	1.61	1.70	1.90	2.52	1.61	1.70	1.90	2.52	ns
LVCMOS25, Fast, 16 mA	0.93	0.94	1.07	1.41	1.61	1.70	1.90	2.52	1.61	1.70	1.90	2.52	ns
LVCMOS25, Fast, 24 mA	0.93	0.94	1.07	1.41	1.61	1.70	1.90	2.52	1.61	1.70	1.90	2.52	ns
LVCMOS18, QUIETIO, 2 mA	1.29	1.30	1.43	1.65	5.97	6.06	6.26	7.28	5.97	6.06	6.26	7.28	ns
LVCMOS18, QUIETIO, 4 mA	1.29	1.30	1.43	1.65	4.79	4.88	5.08	5.90	4.79	4.88	5.08	5.90	ns
LVCMOS18, QUIETIO, 6 mA	1.29	1.30	1.43	1.65	4.10	4.19	4.39	5.16	4.10	4.19	4.39	5.16	ns
LVCMOS18, QUIETIO, 8 mA	1.29	1.30	1.43	1.65	3.76	3.85	4.05	4.84	3.76	3.85	4.05	4.84	ns
LVCMOS18, QUIETIO, 12 mA	1.29	1.30	1.43	1.65	3.40	3.49	3.69	4.41	3.40	3.49	3.69	4.41	ns
LVCMOS18, QUIETIO, 16 mA	1.29	1.30	1.43	1.65	3.25	3.34	3.54	4.23	3.25	3.34	3.54	4.23	ns
LVCMOS18, QUIETIO, 24 mA	1.29	1.30	1.43	1.65	3.01	3.10	3.30	4.06	3.01	3.10	3.30	4.06	ns
LVCMOS18, Slow, 2 mA	1.29	1.30	1.43	1.65	4.67	4.76	4.96	5.86	4.67	4.76	4.96	5.86	ns
LVCMOS18, Slow, 4 mA	1.29	1.30	1.43	1.65	3.74	3.83	4.03	4.83	3.74	3.83	4.03	4.83	ns
LVCMOS18, Slow, 6 mA	1.29	1.30	1.43	1.65	3.05	3.14	3.34	4.10	3.05	3.14	3.34	4.10	ns
LVCMOS18, Slow, 8 mA	1.29	1.30	1.43	1.65	2.24	2.33	2.53	3.21	2.24	2.33	2.53	3.21	ns

Table 27: **IOB Switching Characteristics *(Cont'd)***

I/O Standard	T_{IOPI}				T_{IOOP}				T_{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-4	-3	-2	-1L	-4	-3	-2	-1L	-4	-3	-2	-1L	
LVCMOS18, Slow, 12 mA	1.29	1.30	1.43	1.65	2.04	2.13	2.33	2.91	2.04	2.13	2.33	2.91	ns
LVCMOS18, Slow, 16 mA	1.29	1.30	1.43	1.65	2.04	2.13	2.33	2.91	2.04	2.13	2.33	2.91	ns
LVCMOS18, Slow, 24 mA	1.29	1.30	1.43	1.65	2.04	2.13	2.33	2.85	2.04	2.13	2.33	2.85	ns
LVCMOS18, Fast, 2 mA	1.29	1.30	1.43	1.65	3.64	3.73	3.93	4.76	3.64	3.73	3.93	4.76	ns
LVCMOS18, Fast, 4 mA	1.29	1.30	1.43	1.65	2.44	2.53	2.73	3.45	2.44	2.53	2.73	3.45	ns
LVCMOS18, Fast, 6 mA	1.29	1.30	1.43	1.65	1.93	2.02	2.22	2.72	1.93	2.02	2.22	2.72	ns
LVCMOS18, Fast, 8 mA	1.29	1.30	1.43	1.65	1.86	1.95	2.15	2.67	1.86	1.95	2.15	2.67	ns
LVCMOS18, Fast, 12 mA	1.29	1.30	1.43	1.65	1.76	1.85	2.05	2.57	1.76	1.85	2.05	2.57	ns
LVCMOS18, Fast, 16 mA	1.29	1.30	1.43	1.65	1.76	1.85	2.05	2.57	1.76	1.85	2.05	2.57	ns
LVCMOS18, Fast, 24 mA	1.29	1.30	1.43	1.65	1.76	1.85	2.05	2.57	1.76	1.85	2.05	2.57	ns
LVCMOS18_JEDEC, QUIETIO, 2 mA	1.05	1.06	1.19	1.51	5.96	6.05	6.25	7.23	5.96	6.05	6.25	7.23	ns
LVCMOS18_JEDEC, QUIETIO, 4 mA	1.05	1.06	1.19	1.51	4.80	4.89	5.09	5.90	4.80	4.89	5.09	5.90	ns
LVCMOS18_JEDEC, QUIETIO, 6 mA	1.05	1.06	1.19	1.51	4.09	4.18	4.38	5.15	4.09	4.18	4.38	5.15	ns
LVCMOS18_JEDEC, QUIETIO, 8 mA	1.05	1.06	1.19	1.51	3.76	3.85	4.05	4.83	3.76	3.85	4.05	4.83	ns
LVCMOS18_JEDEC, QUIETIO, 12 mA	1.05	1.06	1.19	1.51	3.40	3.49	3.69	4.41	3.40	3.49	3.69	4.41	ns
LVCMOS18_JEDEC, QUIETIO, 16 mA	1.05	1.06	1.19	1.51	3.25	3.34	3.54	4.23	3.25	3.34	3.54	4.23	ns
LVCMOS18_JEDEC, QUIETIO, 24 mA	1.05	1.06	1.19	1.51	3.01	3.10	3.30	4.06	3.01	3.10	3.30	4.06	ns
LVCMOS18_JEDEC, Slow, 2 mA	1.05	1.06	1.19	1.51	4.64	4.73	4.93	5.85	4.64	4.73	4.93	5.85	ns
LVCMOS18_JEDEC, Slow, 4 mA	1.05	1.06	1.19	1.51	3.74	3.83	4.03	4.80	3.74	3.83	4.03	4.80	ns
LVCMOS18_JEDEC, Slow, 6 mA	1.05	1.06	1.19	1.51	3.05	3.14	3.34	4.10	3.05	3.14	3.34	4.10	ns
LVCMOS18_JEDEC, Slow, 8 mA	1.05	1.06	1.19	1.51	2.24	2.33	2.53	3.21	2.24	2.33	2.53	3.21	ns
LVCMOS18_JEDEC, Slow, 12 mA	1.05	1.06	1.19	1.51	2.04	2.13	2.33	2.91	2.04	2.13	2.33	2.91	ns
LVCMOS18_JEDEC, Slow, 16 mA	1.05	1.06	1.19	1.51	2.04	2.13	2.33	2.91	2.04	2.13	2.33	2.91	ns
LVCMOS18_JEDEC, Slow, 24 mA	1.05	1.06	1.19	1.51	2.04	2.13	2.33	2.85	2.04	2.13	2.33	2.85	ns
LVCMOS18_JEDEC, Fast, 2 mA	1.05	1.06	1.19	1.51	3.62	3.71	3.91	4.74	3.62	3.71	3.91	4.74	ns
LVCMOS18_JEDEC, Fast, 4 mA	1.05	1.06	1.19	1.51	2.44	2.53	2.73	3.44	2.44	2.53	2.73	3.44	ns
LVCMOS18_JEDEC, Fast, 6 mA	1.05	1.06	1.19	1.51	1.93	2.02	2.22	2.70	1.93	2.02	2.22	2.70	ns
LVCMOS18_JEDEC, Fast, 8 mA	1.05	1.06	1.19	1.51	1.85	1.94	2.14	2.66	1.85	1.94	2.14	2.66	ns
LVCMOS18_JEDEC, Fast, 12 mA	1.05	1.06	1.19	1.51	1.77	1.86	2.06	2.57	1.77	1.86	2.06	2.57	ns
LVCMOS18_JEDEC, Fast, 16 mA	1.05	1.06	1.19	1.51	1.77	1.86	2.06	2.57	1.77	1.86	2.06	2.57	ns
LVCMOS18_JEDEC, Fast, 24 mA	1.05	1.06	1.19	1.51	1.77	1.86	2.06	2.57	1.77	1.86	2.06	2.57	ns
LVCMOS15, QUIETIO, 2 mA	1.09	1.10	1.23	1.47	5.52	5.61	5.81	6.75	5.52	5.61	5.81	6.75	ns
LVCMOS15, QUIETIO, 4 mA	1.09	1.10	1.23	1.47	4.66	4.75	4.95	5.78	4.66	4.75	4.95	5.78	ns
LVCMOS15, QUIETIO, 6 mA	1.09	1.10	1.23	1.47	4.12	4.21	4.41	5.19	4.12	4.21	4.41	5.19	ns
LVCMOS15, QUIETIO, 8 mA	1.09	1.10	1.23	1.47	3.96	4.05	4.25	5.00	3.96	4.05	4.25	5.00	ns
LVCMOS15, QUIETIO, 12 mA	1.09	1.10	1.23	1.47	3.58	3.67	3.87	4.67	3.58	3.67	3.87	4.67	ns
LVCMOS15, QUIETIO, 16 mA	1.09	1.10	1.23	1.47	3.37	3.46	3.66	4.43	3.37	3.46	3.66	4.43	ns
LVCMOS15, Slow, 2 mA	1.09	1.10	1.23	1.47	4.23	4.32	4.52	5.38	4.23	4.32	4.52	5.38	ns

Table 27: **IOB Switching Characteristics *(Cont'd)***

I/O Standard	T_{IOPI}				T_{IOOP}				T_{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-4	-3	-2	-1L	-4	-3	-2	-1L	-4	-3	-2	-1L	
LVCMOS15, Slow, 4 mA	1.09	1.10	1.23	1.47	3.47	3.56	3.76	4.54	3.47	3.56	3.76	4.54	ns
LVCMOS15, Slow, 6 mA	1.09	1.10	1.23	1.47	2.34	2.43	2.63	3.26	2.34	2.43	2.63	3.26	ns
LVCMOS15, Slow, 8 mA	1.09	1.10	1.23	1.47	2.35	2.44	2.64	3.28	2.35	2.44	2.64	3.28	ns
LVCMOS15, Slow, 12 mA	1.09	1.10	1.23	1.47	2.08	2.17	2.37	2.98	2.08	2.17	2.37	2.98	ns
LVCMOS15, Slow, 16 mA	1.09	1.10	1.23	1.47	2.06	2.15	2.35	2.97	2.06	2.15	2.35	2.97	ns
LVCMOS15, Fast, 2 mA	1.09	1.10	1.23	1.47	3.34	3.43	3.63	4.41	3.34	3.43	3.63	4.41	ns
LVCMOS15, Fast, 4 mA	1.09	1.10	1.23	1.47	2.32	2.41	2.61	3.28	2.32	2.41	2.61	3.28	ns
LVCMOS15, Fast, 6 mA	1.09	1.10	1.23	1.47	1.83	1.92	2.12	2.60	1.83	1.92	2.12	2.60	ns
LVCMOS15, Fast, 8 mA	1.09	1.10	1.23	1.47	1.78	1.87	2.07	2.57	1.78	1.87	2.07	2.57	ns
LVCMOS15, Fast, 12 mA	1.09	1.10	1.23	1.47	1.78	1.87	2.07	2.49	1.78	1.87	2.07	2.49	ns
LVCMOS15, Fast, 16 mA	1.09	1.10	1.23	1.47	1.78	1.87	2.07	2.46	1.78	1.87	2.07	2.46	ns
LVCMOS15_JEDEC, QUIETIO, 2 mA	1.14	1.15	1.28	1.63	5.54	5.63	5.83	6.74	5.54	5.63	5.83	6.74	ns
LVCMOS15_JEDEC, QUIETIO, 4 mA	1.14	1.15	1.28	1.63	4.66	4.75	4.95	5.76	4.66	4.75	4.95	5.76	ns
LVCMOS15_JEDEC, QUIETIO, 6 mA	1.14	1.15	1.28	1.63	4.12	4.21	4.41	5.19	4.12	4.21	4.41	5.19	ns
LVCMOS15_JEDEC, QUIETIO, 8 mA	1.14	1.15	1.28	1.63	3.97	4.06	4.26	5.02	3.97	4.06	4.26	5.02	ns
LVCMOS15_JEDEC, QUIETIO, 12 mA	1.14	1.15	1.28	1.63	3.59	3.68	3.88	4.67	3.59	3.68	3.88	4.67	ns
LVCMOS15_JEDEC, QUIETIO, 16 mA	1.14	1.15	1.28	1.63	3.38	3.47	3.67	4.43	3.38	3.47	3.67	4.43	ns
LVCMOS15_JEDEC, Slow, 2 mA	1.14	1.15	1.28	1.63	4.23	4.32	4.52	5.39	4.23	4.32	4.52	5.39	ns
LVCMOS15_JEDEC, Slow, 4 mA	1.14	1.15	1.28	1.63	3.47	3.56	3.76	4.54	3.47	3.56	3.76	4.54	ns
LVCMOS15_JEDEC, Slow, 6 mA	1.14	1.15	1.28	1.63	2.34	2.43	2.63	3.27	2.34	2.43	2.63	3.27	ns
LVCMOS15_JEDEC, Slow, 8 mA	1.14	1.15	1.28	1.63	2.35	2.44	2.64	3.28	2.35	2.44	2.64	3.28	ns
LVCMOS15_JEDEC, Slow, 12 mA	1.14	1.15	1.28	1.63	2.06	2.15	2.35	2.97	2.06	2.15	2.35	2.97	ns
LVCMOS15_JEDEC, Slow, 16 mA	1.14	1.15	1.28	1.63	2.06	2.15	2.35	2.97	2.06	2.15	2.35	2.97	ns
LVCMOS15_JEDEC, Fast, 2 mA	1.14	1.15	1.28	1.63	3.33	3.42	3.62	4.41	3.33	3.42	3.62	4.41	ns
LVCMOS15_JEDEC, Fast, 4 mA	1.14	1.15	1.28	1.63	2.32	2.41	2.61	3.29	2.32	2.41	2.61	3.29	ns
LVCMOS15_JEDEC, Fast, 6 mA	1.14	1.15	1.28	1.63	1.83	1.92	2.12	2.58	1.83	1.92	2.12	2.58	ns
LVCMOS15_JEDEC, Fast, 8 mA	1.14	1.15	1.28	1.63	1.78	1.87	2.07	2.57	1.78	1.87	2.07	2.57	ns
LVCMOS15_JEDEC, Fast, 12 mA	1.14	1.15	1.28	1.63	1.78	1.87	2.07	2.50	1.78	1.87	2.07	2.50	ns
LVCMOS15_JEDEC, Fast, 16 mA	1.14	1.15	1.28	1.63	1.78	1.87	2.07	2.46	1.78	1.87	2.07	2.46	ns
LVCMOS12, QUIETIO, 2 mA	1.02	1.03	1.16	1.32	6.45	6.54	6.74	7.67	6.45	6.54	6.74	7.67	ns
LVCMOS12, QUIETIO, 4 mA	1.02	1.03	1.16	1.32	5.03	5.12	5.32	6.18	5.03	5.12	5.32	6.18	ns
LVCMOS12, QUIETIO, 6 mA	1.02	1.03	1.16	1.32	4.70	4.79	4.99	5.81	4.70	4.79	4.99	5.81	ns
LVCMOS12, QUIETIO, 8 mA	1.02	1.03	1.16	1.32	4.28	4.37	4.57	5.45	4.28	4.37	4.57	5.45	ns
LVCMOS12, QUIETIO, 12 mA	1.02	1.03	1.16	1.32	4.03	4.12	4.32	5.16	4.03	4.12	4.32	5.16	ns
LVCMOS12, Slow, 2 mA	1.02	1.03	1.16	1.32	5.03	5.12	5.32	6.22	5.03	5.12	5.32	6.22	ns
LVCMOS12, Slow, 4 mA	1.02	1.03	1.16	1.32	2.89	2.98	3.18	3.93	2.89	2.98	3.18	3.93	ns
LVCMOS12, Slow, 6 mA	1.02	1.03	1.16	1.32	2.82	2.91	3.11	3.81	2.82	2.91	3.11	3.81	ns
LVCMOS12, Slow, 8 mA	1.02	1.03	1.16	1.32	2.39	2.48	2.68	3.34	2.39	2.48	2.68	3.34	ns

Table 27: **IOB Switching Characteristics *(Cont'd)***

I/O Standard	T_{IOPI}				T_{IOOP}				T_{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-4	-3	-2	-1L	-4	-3	-2	-1L	-4	-3	-2	-1L	
LVCMOS12, Slow, 12 mA	1.02	1.03	1.16	1.32	2.13	2.22	2.42	3.09	2.13	2.22	2.42	3.09	ns
LVCMOS12, Fast, 2 mA	1.02	1.03	1.16	1.32	3.51	3.60	3.80	4.61	3.51	3.60	3.80	4.61	ns
LVCMOS12, Fast, 4 mA	1.02	1.03	1.16	1.32	2.40	2.49	2.69	3.38	2.40	2.49	2.69	3.38	ns
LVCMOS12, Fast, 6 mA	1.02	1.03	1.16	1.32	1.84	1.93	2.13	2.70	1.84	1.93	2.13	2.70	ns
LVCMOS12, Fast, 8 mA	1.02	1.03	1.16	1.32	1.73	1.82	2.02	2.60	1.73	1.82	2.02	2.60	ns
LVCMOS12, Fast, 12 mA	1.02	1.03	1.16	1.32	1.71	1.80	2.00	2.50	1.71	1.80	2.00	2.50	ns
LVCMOS12_JEDEC, QUIETIO, 2 mA	1.61	1.62	1.75	2.00	6.44	6.53	6.73	7.67	6.44	6.53	6.73	7.67	ns
LVCMOS12_JEDEC, QUIETIO, 4 mA	1.61	1.62	1.75	2.00	5.03	5.12	5.32	6.18	5.03	5.12	5.32	6.18	ns
LVCMOS12_JEDEC, QUIETIO, 6 mA	1.61	1.62	1.75	2.00	4.72	4.81	5.01	5.80	4.72	4.81	5.01	5.80	ns
LVCMOS12_JEDEC, QUIETIO, 8 mA	1.61	1.62	1.75	2.00	4.28	4.37	4.57	5.43	4.28	4.37	4.57	5.43	ns
LVCMOS12_JEDEC, QUIETIO, 12 mA	1.61	1.62	1.75	2.00	4.04	4.13	4.33	5.16	4.04	4.13	4.33	5.16	ns
LVCMOS12_JEDEC, Slow, 2 mA	1.61	1.62	1.75	2.00	5.05	5.14	5.34	6.23	5.05	5.14	5.34	6.23	ns
LVCMOS12_JEDEC, Slow, 4 mA	1.61	1.62	1.75	2.00	2.90	2.99	3.19	3.93	2.90	2.99	3.19	3.93	ns
LVCMOS12_JEDEC, Slow, 6 mA	1.61	1.62	1.75	2.00	2.81	2.90	3.10	3.81	2.81	2.90	3.10	3.81	ns
LVCMOS12_JEDEC, Slow, 8 mA	1.61	1.62	1.75	2.00	2.40	2.49	2.69	3.34	2.40	2.49	2.69	3.34	ns
LVCMOS12_JEDEC, Slow, 12 mA	1.61	1.62	1.75	2.00	2.14	2.23	2.43	3.09	2.14	2.23	2.43	3.09	ns
LVCMOS12_JEDEC, Fast, 2 mA	1.61	1.62	1.75	2.00	3.51	3.60	3.80	4.62	3.51	3.60	3.80	4.62	ns
LVCMOS12_JEDEC, Fast, 4 mA	1.61	1.62	1.75	2.00	2.40	2.49	2.69	3.38	2.40	2.49	2.69	3.38	ns
LVCMOS12_JEDEC, Fast, 6 mA	1.61	1.62	1.75	2.00	1.84	1.93	2.13	2.70	1.84	1.93	2.13	2.70	ns
LVCMOS12_JEDEC, Fast, 8 mA	1.61	1.62	1.75	2.00	1.74	1.83	2.03	2.60	1.74	1.83	2.03	2.60	ns
LVCMOS12_JEDEC, Fast, 12 mA	1.61	1.62	1.75	2.00	1.71	1.80	2.00	2.50	1.71	1.80	2.00	2.50	ns

Table 28: **IOB 3-state ON Output Switching Characteristics (T_{IOTPHZ})**

Symbol	Description	Speed Grade				Units
		-4	-3	-2	-1L	
T_{IOTPHZ}	T input to Pad high-impedance	1.39	1.59	1.59	1.91	ns

I/O Standard Adjustment Measurement Methodology

Input Delay Measurements

Table 29 shows the test setup parameters used for measuring input delay.

Table 29: **Input Delay Measurement Methodology**

Description	I/O Standard Attribute	V_L (1)	V_H (1)	V_{MEAS} (3,4)	V_{REF} (2,4)
LVTTL (Low-Voltage Transistor-Transistor Logic)	LVTTL	0	3.0	1.4	–
LVCMOS (Low-Voltage CMOS), 3.3V	LVCMOS33	0	3.3	1.65	–
LVCMOS, 2.5V	LVCMOS25	0	2.5	1.25	–
LVCMOS, 1.8V	LVCMOS18	0	1.8	0.9	–
LVCMOS, 1.5V	LVCMOS15	0	1.5	0.75	–
LVCMOS, 1.2V	LVCMOS12	0	1.2	0.6	–
PCI (Peripheral Component Interface), 33 MHz and 66 MHz, 3.3V	PCI33_3, PCI66_3	Per PCI Specification			–
HSTL (High-Speed Transceiver Logic), Class I & II	HSTL_I, HSTL_II	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.75
HSTL, Class III	HSTL_III	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.90
HSTL, Class I & II, 1.8V	HSTL_I_18, HSTL_II_18	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.90
HSTL, Class III 1.8V	HSTL_III_18	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	1.1
SSTL (Stub Terminated Transceiver Logic), Class I & II, 3.3V	SSTL3_I, SSTL3_II	V_{REF} – 0.75	V_{REF} + 0.75	V_{REF}	1.5
SSTL, Class I & II, 2.5V	SSTL2_I, SSTL2_II	V_{REF} – 0.75	V_{REF} + 0.75	V_{REF}	1.25
SSTL, Class I & II, 1.8V	SSTL18_I, SSTL18_II	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.90
SSTL, Class II, 1.5V	SSTL15_II	V_{REF} – 0.2	V_{REF} + 0.2	V_{REF}	0.75
LVDS (Low-Voltage Differential Signaling), 2.5V & 3.3V	LVDS_25, LVDS_33	1.25 – 0.125	1.25 + 0.125	0(5)	–
LVPECL (Low-Voltage Positive Emitter-Coupled Logic), 2.5V & 3.3V	LVPECL_25, LVPECL_33	1.2 – 0.3	1.2 – 0.3	0(5)	–
BLVDS (Bus LVDS), 2.5V	BLVDS_25	1.3 – 0.125	1.3 + 0.125	0(5)	–
Mini-LVDS, 2.5V & 3.3V	MINI_LVDS_25, MINI_LVDS_33	1.2 – 0.125	1.2 + 0.125	0(5)	–
RSDS (Reduced Swing Differential Signaling), 2.5V & 3.3V	RSDS_25, RSDS_33	1.2 – 0.1	1.2 + 0.1	0(5)	–
TMDS (Transition Minimized Differential Signaling), 3.3V	TMDS_33	3.0 – 0.1	3.0 + 0.1	0(5)	–
PPDS (Point-to-Point Differential Signaling, 2.5V & 3.3V	PPDS_25, PPDS_33	1.25 – 0.1	1.25 + 0.1	0(5)	–

Notes:

1. Input waveform switches between V_L and V_H.
2. Measurements are made at typical, minimum, and maximum V_{REF} values. Reported delays reflect worst case of these measurements. V_{REF} values listed are typical.
3. Input voltage level from which measurement starts.
4. This is an input voltage reference that bears no relation to the V_{REF} / V_{MEAS} parameters found in IBIS models and/or noted in Figure 4.
5. The value given is the differential input voltage.

Output Delay Measurements

Output delays are measured using a Tektronix P6245 TDS500/600 probe (< 1 pF) across approximately 4" of FR4 microstrip trace. Standard termination was used for all testing. The propagation delay of the 4" trace is characterized separately and subtracted from the final measurement, and is therefore not included in the generalized test setups shown in Figure 4 and Figure 5.

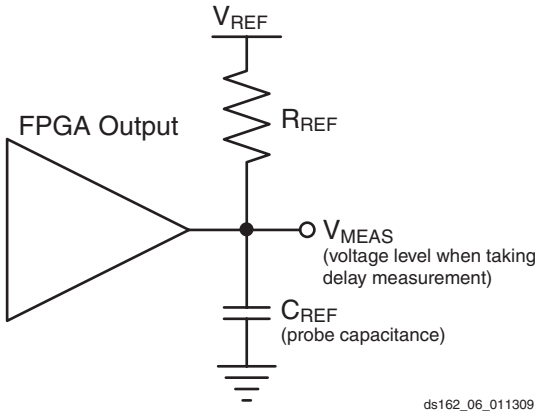

Figure 4: **Single-Ended Test Setup**

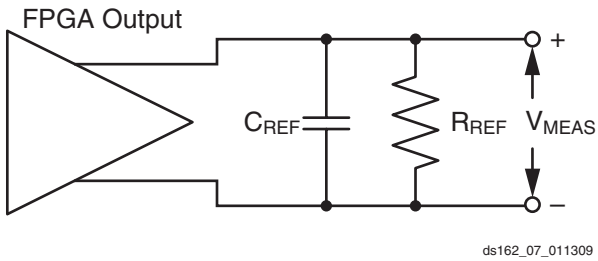

Figure 5: **Differential Test Setup**

Measurements and test conditions are reflected in the IBIS models except where the IBIS format precludes it. Parameters V_{REF}, R_{REF}, C_{REF}, and V_{MEAS} fully describe the test conditions for each I/O standard. The most accurate prediction of propagation delay in any given application can be obtained through IBIS simulation, using the following method:

1. Simulate the output driver of choice into the generalized test setup, using values from Table 30.
2. Record the time to V_{MEAS}.
3. Simulate the output driver of choice into the actual PCB trace and load, using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to V_{MEAS}.
5. Compare the results of steps 2 and 4. The increase or decrease in delay yields the actual propagation delay of the PCB trace.

Table 30: **Output Delay Measurement Methodology**

Description	I/O Standard Attribute	R_{REF} (Ω)	C_{REF}[1] (pF)	V_{MEAS} (V)	V_{REF} (V)
LVTTL (Low-Voltage Transistor-Transistor Logic)	LVTTL (all)	1M	0	1.4	0
LVCMOS (Low-Voltage CMOS), 3.3V	LVCMOS33	1M	0	1.65	0
LVCMOS, 2.5V	LVCMOS25	1M	0	1.25	0
LVCMOS, 1.8V	LVCMOS18	1M	0	0.9	0
LVCMOS, 1.5V	LVCMOS15	1M	0	0.75	0
LVCMOS, 1.2V	LVCMOS12	1M	0	0.75	0
PCI (Peripheral Component Interface) 33 MHz and 66 MHz, 3.3V	PCI33_3, PCI66_3 (rising edge)	25	10[2]	0.94	0
	PCI33_3, PCI66_3 (falling edge)	25	10[2]	2.03	3.3
HSTL (High-Speed Transceiver Logic), Class I	HSTL_I	50	0	V_{REF}	0.75
HSTL, Class II	HSTL_II	25	0	V_{REF}	0.75
HSTL, Class III	HSTL_III	50	0	0.9	1.5
HSTL, Class I, 1.8V	HSTL_I_18	50	0	V_{REF}	0.9
HSTL, Class II, 1.8V	HSTL_II_18	25	0	V_{REF}	0.9
HSTL, Class III, 1.8V	HSTL_III_18	50	0	1.1	1.8
SSTL (Stub Series Terminated Logic), Class I, 1.8V	SSTL18_I	50	0	V_{REF}	0.9
SSTL, Class II, 1.8V	SSTL18_II	25	0	V_{REF}	0.9
SSTL, Class I, 2.5V	SSTL2_I	50	0	V_{REF}	1.25

Table 30: **Output Delay Measurement Methodology *(Cont'd)***

Description	I/O Standard Attribute	R_{REF} (Ω)	C_{REF}[1] (pF)	V_{MEAS} (V)	V_{REF} (V)
SSTL, Class II, 2.5V	SSTL2_II	25	0	V_{REF}	1.25
SSTL, Class II, 1.5V	SSTL15_II	25	0	V_{REF}	0.75
LVDS (Low-Voltage Differential Signaling), 2.5V & 3.3V	LVDS_25, LVDS_33	100	0	0[3]	1.2
BLVDS (Bus LVDS), 2.5V	BLVDS_25	100	0	0[3]	0
Mini-LVDS, 2.5V & 3.3V	MINI_LVDS_25, MINI_LVDS_33	100	0	0[3]	1.2
RSDS (Reduced Swing Differential Signaling), 2.5V & 3.3V	RSDS_25, RSDS_33	100	0	0[3]	1.2
TMDS (Transition Minimized Differential Signaling), 3.3V	TMDS_33	100	0	0[3]	
PPDS (Point-to-Point Differential Signaling, 2.5V & 3.3V	PPDS_25, PPDS_33	100	0	0[3]	–

Notes:
1. C_{REF} is the capacitance of the probe, nominally 0 pF.
2. Per PCI specifications.
3. The value given is the differential output voltage.

Simultaneously Switching Outputs

Due to lead inductance, a given package supports a limited number of simultaneous switching outputs (SSOs) when using fast, high-drive outputs. Table 31 and Table 32 provide guidelines for the recommended maximum allowable number of SSOs. These guidelines describe the maximum number of user I/O pins of an output signal standard that should simultaneously switch in the same direction, while maintaining a safe level of switching noise. Meeting these guidelines for the stated test conditions ensures that the FPGA operates free from the adverse effects of GND and power bounce.

For each device/package combination, Table 31 provides the number of equivalent V_{CCO}/GND pairs per bank. For each output signal standard and drive strength, Table 32 recommends the maximum number of SSOs, switching in the same direction, allowed per V_{CCO}/GND pair within an I/O bank. The guidelines are categorized by package style, slew rate, and output drive current. The number of SSOs are also specified by I/O bank. Multiply the appropriate numbers from each table to calculate the maximum number of SSOs allowed within an I/O bank. Exceeding these SSO guidelines can result in increased power or GND bounce, degraded signal integrity, or increased system jitter.

The recommended maximum SSO values assume that the FPGA is soldered on a printed circuit board and that the board uses sound design practices. Due to the additional lead inductance introduced by the socket, the SSO values do not apply for FPGAs mounted in sockets. The SSO values assume that the V_{CCAUX} is powered at 3.3V. Setting V_{CCAUX} to 2.5V provides better SSO characteristics. For more detail, see the *Spartan-6 FPGA SelectIO Resources User Guide*.

Table 31: **Spartan-6 FPGA V_{CCO}/GND Pairs per Bank**

Package	Devices	Description	Bank 0	Bank 1	Bank 2	Bank 3	Bank 4	Bank 5
TQG144	LX	V_{CCO}/GND Pairs	3	3	2	3	N/A	N/A
		I/O per Pair	8	8	13	8	N/A	N/A
CPG196	LX	VCCO/GND Pairs	4	6	4	6	N/A	N/A
		I/O per Pair	6	4	7	4	N/A	N/A
CSG225	LX	V_{CCO}/GND Pairs	4	4	4	4	N/A	N/A
		I/O per Pair	8	8	8	8	N/A	N/A
FT(G)256	LX	V_{CCO}/GND Pairs	5	6	4	5	N/A	N/A
		I/O per Pair	8	9	9	10	N/A	N/A
CSG324	LX	V_{CCO}/GND Pairs	6	6	6	6	N/A	N/A
		I/O per Pair	7	9	7	9	N/A	N/A
	LXT	V_{CCO}/GND Pairs	4	6	6	6	N/A	N/A
		I/O per Pair	4	9	10	9	N/A	N/A

Table 31: **Spartan-6 FPGA V_{CCO}/GND Pairs per Bank *(Cont'd)***

Package	Devices	Description	Bank 0	Bank 1	Bank 2	Bank 3	Bank 4	Bank 5
CSG484	LX	V_{CCO}/GND Pairs	8	13	8	13	N/A	N/A
		I/O per Pair	5	8	7	8	N/A	N/A
	LXT	V_{CCO}/GND Pairs	7	12	8	13	N/A	N/A
		I/O per Pair	5	8	6	8	N/A	N/A
FG(G)484	LX	V_{CCO}/GND Pairs	10	10	11	11	N/A	N/A
		I/O per Pair	5	6	7	5	N/A	N/A
	LXT	V_{CCO}/GND Pairs	6	10	11	10	N/A	N/A
		I/O per Pair	7	6	6	6	N/A	N/A
FG(G)676	LX45	V_{CCO}/GND Pairs	12	15	10	16	N/A	N/A
		I/O per Pair	3	7	8	7	N/A	N/A
	LX75, LX100, LX150	V_{CCO}/GND Pairs	12	9	10	10	6	6
		I/O per Pair	4	10	5	9	8	9
	LXT	V_{CCO}/GND Pairs	10	8	10	8	7	7
		I/O per Pair	5	7	5	8	7	7
FG(G)900	LX	V_{CCO}/GND Pairs	17	14	17	14	7	8
		I/O per Pair	7	6	7	8	7	6
	LXT	V_{CCO}/GND Pairs	15	14	13	14	7	8
		I/O per Pair	6	6	7	8	7	6

Table 32: **SSO Limit per V_{CCO}/GND Pair for CSG324 and FG(G)484 Packages**

V_{CCO}	I/O Standard	Drive	Slew	SSO Limit per V_{CCO}/GND Pair			
				CSG324		FG(G)484	
				Bank 0/2	Bank 1/3	Bank 0/2	Bank 1/3
1.2V	LVCMOS12, LVCMOS12_JEDEC	2	Fast	57 (1)	35	30	35
			Slow	88	55	51	52
			QuietIO	88	58	71	70
		4	Fast	30	20	17	19
			Slow	46	25	23	22
			QuietIO	47	32	35	32
		6	Fast	22	15	13	14
			Slow	36	20	19	17
			QuietIO	36	24	26	24
		8	Fast	N/A	12	N/A	12
			Slow	N/A	15	N/A	13
			QuietIO	N/A	20	N/A	19
		12	Fast	N/A	3	N/A	2
			Slow	N/A	8	N/A	5
			QuietIO	N/A	11	N/A	10

Table 32: **SSO Limit per V_{CCO}/GND Pair for CSG324 and FG(G)484 Packages *(Cont'd)***

V_{CCO}	I/O Standard	Drive	Slew	SSO Limit per V_{CCO}/GND Pair			
				CSG324		FG(G)484	
				Bank 0/2	Bank 1/3	Bank 0/2	Bank 1/3
1.5V	LVCMOS15, LVCMOS15_JEDEC	2	Fast	66	40	33	41
			Slow	100	62	57	56
			QuietIO	100	67	70	66
		4	Fast	34	21	19	21
			Slow	54	30	30	24
			QuietIO	54	33	38	30
		6	Fast	24	16	14	16
			Slow	36	19	18	17
			QuietIO	39	24	27	21
		8	Fast	20	13	11	12
			Slow	32	16	16	14
			QuietIO	32	20	23	17
		12	Fast	N/A	5	N/A	3
			Slow	N/A	8	N/A	5
			QuietIO	N/A	10	N/A	9
		16	Fast	N/A	3	N/A	3
			Slow	N/A	8	N/A	5
			QuietIO	N/A	10	N/A	9
	HSTL_I (3)			15	10	9	10
	HSTL_II (3)			N/A	5	N/A	3
	HSTL_III (3)			17	9	7	9
	SSTL_15_II (3)			N/A	3	N/A	2

Table 32: **SSO Limit per V_{CCO}/GND Pair for CSG324 and FG(G)484 Packages *(Cont'd)***

V_{CCO}	I/O Standard	Drive	Slew	SSO Limit per V_{CCO}/GND Pair			
				CSG324		FG(G)484	
				Bank 0/2	Bank 1/3	Bank 0/2	Bank 1/3
1.8V	LVCMOS18, LVCMOS18_JEDEC	2	Fast	74	46	39	47
			Slow	112	75	65	74
			QuietIO	112	80	80	85
		4	Fast	41	25	22	25
			Slow	65	36	38	29
			QuietIO	65	40	45	35
		6	Fast	28	18	16	17
			Slow	46	25	27	19
			QuietIO	46	28	30	23
		8	Fast	23	15	13	14
			Slow	32	18	16	16
			QuietIO	37	22	25	18
		12	Fast	10	5	3	3
			Slow	15	8	7	5
			QuietIO	19	10	11	8
		16	Fast	10	5	3	3
			Slow	15	8	7	5
			QuietIO	19	10	11	8
		24	Fast	N/A	3	N/A	2
			Slow	N/A	7	N/A	5
			QuietIO	N/A	10	N/A	8
	HSTL_I_18 (3)			15	10	9	9
	HSTL_II_18 (3)			N/A	5	N/A	4
	HSTL_III_18 (3)			16	10	9	11
	MOBILE_DDR			23	14	12	14
	SSTL_18_I (3)			16	10	9	10
	SSTL_18_II (3)			N/A	5	N/A	3

Table 32: **SSO Limit per V_{CCO}/GND Pair for CSG324 and FG(G)484 Packages *(Cont'd)***

V_{CCO}	I/O Standard	Drive	Slew	SSO Limit per V_{CCO}/GND Pair			
				CSG324		FG(G)484	
				Bank 0/2	Bank 1/3	Bank 0/2	Bank 1/3
2.5V	LVCMOS25	2	Fast	71	43	38	43
			Slow	92	52	46	48
			QuietIO	99	64	57	59
		4	Fast	38	24	21	23
			Slow	52	31	26	27
			QuietIO	55	32	33	30
		6	Fast	27	17	15	16
			Slow	41	22	19	19
			QuietIO	41	23	25	19
		8	Fast	24	15	12	14
			Slow	36	18	15	16
			QuietIO	37	19	21	16
		12	Fast	9	3	1	1
			Slow	11	5	2	2
			QuietIO	16	8	3	5
		16	Fast	9	3	1	1
			Slow	11	5	1	2
			QuietIO	16	8	4	5
		24	Fast	N/A	3	N/A	1
			Slow	N/A	5	N/A	1
			QuietIO	N/A	8	N/A	5
	SSTL_2_I (3)			18	11	10	11
	SSTL_2_II (3)			N/A	7	N/A	7

Table 32: **SSO Limit per V_{CCO}/GND Pair for CSG324 and FG(G)484 Packages *(Cont'd)***

V_{CCO}	I/O Standard	Drive	Slew	SSO Limit per V_{CCO}/GND Pair			
				CSG324		FG(G)484	
				Bank 0/2	Bank 1/3	Bank 0/2	Bank 1/3
3.3V	LVCMOS33	2	Fast	75	46	42	44
			Slow	96	55	50	49
			QuietIO	107	68	60	60
		4	Fast	47	27	21	25
			Slow	62	37	32	32
			QuietIO	66	42	39	37
		6	Fast	33	19	14	17
			Slow	45	25	19	22
			QuietIO	51	30	29	25
		8	Fast	27	15	11	14
			Slow	38	20	15	18
			QuietIO	45	24	25	20
		12	Fast	5	2	1	1
			Slow	10	5	1	1
			QuietIO	15	9	2	7
		16	Fast	5	2	1	1
			Slow	10	5	1	1
			QuietIO	15	10	3	8
		24	Fast	7	2	1	1
			Slow	12	3	1	1
			QuietIO	19	9	7	3

Table 32: **SSO Limit per V_{CCO}/GND Pair for CSG324 and FG(G)484 Packages *(Cont'd)***

V_{CCO}	I/O Standard	Drive	Slew	SSO Limit per V_{CCO}/GND Pair			
				CSG324		FG(G)484	
				Bank 0/2	Bank 1/3	Bank 0/2	Bank 1/3
3.3V	LVTTL	2	Fast	105	65	53	62
			Slow	137	80	70	73
			QuietIO	147	89	79	91
		4	Fast	55	30	23	27
			Slow	76	41	34	37
			QuietIO	79	49	44	46
		6	Fast	39	21	16	20
			Slow	54	28	21	25
			QuietIO	62	39	34	34
		8	Fast	28	16	12	15
			Slow	40	22	16	19
			QuietIO	50	28	27	24
		12	Fast	5	2	1	1
			Slow	11	5	1	1
			QuietIO	15	10	2	8
		16	Fast	5	2	1	1
			Slow	11	5	1	1
			QuietIO	17	11	3	8
		24	Fast	7	2	1	1
			Slow	13	3	3	1
			QuietIO	21	9	8	4
	PCI33_3			35	19	18	19
	PCI66_3			35	19	18	19
	SSTL_3_I (3)			13	8	5	7
	SSTL_3_II (3)			9	3	2	2
	SDIO			34	18	17	15

Notes:

1. SSO limits greater than the number of I/O per V_{CCO}/GND pair (Table 31) indicate No Limit for the given I/O standard. They are provided in this table to calculate limits when using multiple I/O standards in a bank.
2. Not available (N/A) indicates that the I/O standard is not available in the given bank.
3. For differential versions of these standards, each differential pair is equivalent to one single-ended pin.

Input/Output Logic Switching Characteristics

Table 33: **ILOGIC2 Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-4	-3	-2	-1L	
Setup/Hold						
T_{ICE0CK}/T_{ICKCE0}	CE0 pin Setup/Hold with respect to CLK	0.60 –0.35	0.60 –0.25	0.79 –0.22	1.28 –0.55	ns
T_{ISRCK}/T_{ICKSR}	SR pin Setup/Hold with respect to CLK	0.79 –0.28	0.79 –0.22	0.98 –0.20	1.35 –0.49	ns
T_{IDOCK}/T_{IOCKD}	D pin Setup/Hold with respect to CLK without Delay	1.37 –1.00	1.37 –0.87	1.73 –0.87	1.97 –1.09	ns
T_{IDOCKD}/T_{IOCKDD}	DDLY pin Setup/Hold with respect to CLK (using IODELAY2)	0.47 –0.15	0.47 –0.03	0.54 –0.02	0.64 –0.16	ns
Combinatorial						
T_{IDI}	D pin to O pin propagation delay, no Delay	1.25	1.28	1.53	1.97	ns
T_{IDID}	DDLY pin to O pin propagation delay (using IODELAY2)	0.34	0.39	0.44	0.64	ns
Sequential Delays						
T_{IDLO}	D pin to Q pin using flip-flop as a latch without Delay	1.96	1.86	2.39	3.22	ns
T_{IDLOD}	DDLY pin to Q1 pin using flip-flop as a latch (using IODELAY2)	1.06	0.97	1.20	1.89	ns
T_{ICKQ}	CLK to Q outputs	0.98	1.24	1.43	1.66	ns
$T_{RQ\_ILOGIC2}$	SR pin to Q outputs	1.81	1.81	2.50	3.05	ns

Table 34: **OLOGIC2 Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-4	-3	-2	-1L	
Setup/Hold						
T_{ODCK}/T_{OCKD}	D1/D2 pins Setup/Hold with respect to CLK	0.66 –0.14	0.67 –0.05	0.97 0.00	1.16 –0.26	ns
T_{OOCECK}/T_{OCKOCE}	OCE pin Setup/Hold with respect to CLK	0.84 –0.19	0.84 –0.10	1.01 –0.05	0.56 –0.22	ns
T_{OSRCK}/T_{OCKSR}	SR pin Setup/Hold with respect to CLK	0.77 –0.37	0.79 –0.28	1.03 –0.23	1.09 –0.46	ns
T_{OTCK}/T_{OCKT}	T1/T2 pins Setup/Hold with respect to CLK	0.61 –0.16	0.63 –0.16	0.82 –0.16	0.86 –0.18	ns
T_{OTCECK}/T_{OCKTCE}	TCE pin Setup/Hold with respect to CLK	0.54 –0.15	0.74 –0.06	0.93 –0.01	0.47 –0.12	ns
Sequential Delays						
T_{OCKQ}	CLK to OQ/TQ out	0.51	0.51	0.74	0.97	ns
$T_{RQ\_OLOGIC2}$	SR pin to OQ/TQ out	1.81	1.81	2.50	3.05	ns

Input Serializer/Deserializer Switching Characteristics

Table 35: **ISERDES2 Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-4	-3	-2	-1L	
Setup/Hold for Control Lines						
$T_{ISCCK\_BITSLIP}$/ $T_{ISCKC\_BITSLIP}$	BITSLIP pin Setup/Hold with respect to CLKDIV	0.16 –0.09	0.20 –0.09	0.31 –0.09	0.34 –0.14	ns
T_{ISCCK_CE} / T_{ISCKC_CE}	CE pin Setup/Hold with respect to CLK	0.71 –0.47	0.71 –0.42	0.97 –0.42	1.39 –0.71	ns
Setup/Hold for Data Lines						
T_{ISDCK_D} /T_{ISCKD_D}	D pin Setup/Hold with respect to CLK	0.24 –0.05	0.25 –0.05	0.29 –0.05	0.12 –0.06	ns
T_{ISDCK_DDLY} /T_{ISCKD_DDLY}	DDLY pin Setup/Hold with respect to CLK (using IODELAY2)	–0.25 0.30	–0.25 0.42	–0.25 0.56	–0.54 0.67	ns
$T_{ISDCK\_D\_DDR}$ /$T_{ISCKD\_D\_DDR}$	D pin Setup/Hold with respect to CLK at DDR mode	–0.03 0.04	–0.03 0.16	–0.03 0.18	–0.05 0.12	ns
$T_{ISDCK\_DDLY\_DDR}$/ $T_{ISCKD\_DDLY\_DDR}$	D pin Setup/Hold with respect to CLK at DDR mode (using IODELAY2)	–0.40 0.48	–0.40 0.53	–0.40 0.71	–0.71 0.86	ns
Sequential Delays						
T_{ISCKO_Q}	CLKDIV to out at Q pin	1.30	1.44	2.02	2.22	ns

Output Serializer/Deserializer Switching Characteristics

Table 36: **OSERDES2 Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-4	-3	-2	-1L	
Setup/Hold						
T_{OSDCK_D}/T_{OSCKD_D}	D input Setup/Hold with respect to CLKDIV	–0.03 1.02	–0.03 1.17	–0.03 1.27	–0.02 0.23	ns
T_{OSDCK_T}/T_{OSCKD_T}(1)	T input Setup/Hold with respect to CLK	–0.05 1.03	–0.05 1.13	–0.05 1.23	–0.05 0.24	ns
T_{OSCCK_OCE}/T_{OSCKC_OCE}	OCE input Setup/Hold with respect to CLK	0.12 –0.03	0.15 –0.03	0.24 –0.03	0.28 –0.17	ns
T_{OSCCK_TCE}/T_{OSCKC_TCE}	TCE input Setup/Hold with respect to CLK	0.14 –0.08	0.17 –0.08	0.27 –0.08	0.31 –0.16	ns
Sequential Delays						
T_{OSCKO_OQ}	Clock to out from CLK to OQ	0.94	1.11	1.51	1.89	ns
T_{OSCKO_TQ}	Clock to out from CLK to TQ	0.94	1.11	1.51	1.91	ns

Notes:
1. T_{OSDCK_T2}/T_{OSCKD_T2} (T input setup/hold with respect to CLKDIV) are reported as T_{OSDCK_T}/T_{OSCKD_T} in TRACE report.

Input/Output Delay Switching Characteristics

Table 37: **IODELAY2 Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-4	-3	-2	-1L	
T_{IODCCK_CAL} / T_{IODCKC_CAL}	CAL pin Setup/Hold with respect to CK	0.28 –0.13	0.33 –0.13	0.48 –0.13	0.57 –0.24	ns
T_{IODCCK_CE} / T_{IODCKC_CE}	CE pin Setup/Hold with respect to CK	0.14 –0.03	0.17 –0.03	0.25 –0.02	0.33 0.01	ns
T_{IODCCK_INC}/ T_{IODCKC_INC}	INC pin Setup/Hold with respect to CK	0.10 0.02	0.12 0.03	0.18 0.06	0.23 0.11	ns
T_{IODCCK_RST}/ T_{IODCKC_RST}	RST pin Setup/Hold with respect to CK	0.12 –0.02	0.15 –0.02	0.22 –0.01	0.28 0.02	ns
T_{TAP1} (2)	Maximum tap 1 delay			16		ps
T_{TAP2}	Maximum tap 2 delay			77		ps
T_{TAP3}	Maximum tap 3 delay			140		ps
T_{TAP4}	Maximum tap 4 delay			166		ps
T_{TAP5}	Maximum tap 5 delay			231		ps
T_{TAP6}	Maximum tap 6 delay			292		ps
T_{TAP7}	Maximum tap 7 delay			343		ps
T_{TAP8}	Maximum tap 8 delay			424		ps
F_{MINCAL}	Minimum allowed bit rate for calibration in variable mode: VARIABLE_FROM_ZERO, VARIABLE_FROM_HALF_MAX, and DIFF_PHASE_DETECTOR.			188		Mb/s
$T_{IODDO\_IDATAIN}$	Propagation delay through IODELAY2	Note 1	Note 1	Note 1	Note 1	
$T_{IODDO\_ODATAIN}$	Propagation delay through IODELAY2	Note 1	Note 1	Note 1	Note 1	

Notes:
1. Delay depends on IODELAY2 tap setting. See TRACE report for actual values.
2. Maximum delay = integer(number of taps/8) × T_{TAP8} + T_{TAPn} (where n equals the remainder). For minimum delay consult the TRACE setup and hold report.

CLB Switching Characteristics (SLICEM Only)

Table 38: **CLB Switching Characteristics (SLICEM Only)**

Symbol	Description	Speed Grade				Units
		-4	-3	-2	-1L	
Combinatorial Delays						
T_{ILO}	An – Dn LUT inputs to A to D outputs	0.26	0.26	0.38	0.54	ns, Max
	An – Dn LUT inputs through F7AMUX/F7BMUX to AMUX/CMUX output	0.43	0.43	0.61	0.84	ns, Max
T_{OPAB}	An – Dn LUT inputs through F7AMUX or F7BMUX and F8MUX to BMUX output	0.46	0.46	0.65	0.90	ns, Max
T_{ITO}	An – Dn LUT inputs through latch to AQ – DQ outputs	0.88	0.95	1.28	1.63	ns, Max
T_{TITO_LOGIC}	An – Dn LUT inputs to AQ – DQ outputs (latch as logic)	0.88	0.95	1.28	1.63	ns, Max
T_{OPCYA}	An LUT inputs to COUT output	0.48	0.48	0.72	0.98	ns, Max
T_{OPCYB}	Bn LUT inputs to COUT output	0.48	0.49	0.71	0.95	ns, Max
T_{OPCYC}	Cn LUT inputs to COUT output	0.33	0.33	0.49	0.71	ns, Max
T_{OPCYD}	Dn LUT inputs to COUT output	0.35	0.35	0.48	0.71	ns, Max
T_{AXCY}	AX input to COUT output	0.25	0.26	0.40	0.45	ns, Max
T_{BXCY}	BX input to COUT output	0.15	0.16	0.24	0.31	ns, Max
T_{CXCY}	CX input to COUT output	0.09	0.12	0.18	0.15	ns, Max
T_{DXCY}	DX input to COUT output	0.10	0.11	0.14	0.20	ns, Max
T_{BYP}	CIN input to COUT output	0.08	0.10	0.13	0.12	ns, Max
T_{CINA}	CIN input to AMUX output	0.22	0.22	0.29	0.48	ns, Max
T_{CINB}	CIN input to BMUX output	0.31	0.31	0.46	0.59	ns, Max
T_{CINC}	CIN input to CMUX output	0.31	0.31	0.41	0.60	ns, Max
T_{CIND}	CIN input to DMUX output	0.32	0.32	0.44	0.68	ns, Max
Sequential Delays						
T_{CKO}	Clock to AQ – DQ outputs	0.43	0.53	0.64	0.81	ns, Max
Setup and Hold Times of CLB Flip-Flops Before/After Clock CLK						
T_{DICK}/T_{CKDI}	AX – DX input to CLK on A – D flip-flops	0.47 0.27	0.47 0.39	0.74 0.54	0.95 0.65	ns, Min
T_{CECK}/T_{CKCE}	CE input to CLK on A – D flip-flops	0.31 –0.07	0.37 –0.07	0.59 –0.07	0.59 –0.17	ns, Min
T_{SRCK}/T_{CKSR}	SR input to CLK on A – D flip-flops	0.41 –0.05	0.42 0.01	0.49 0.01	0.63 –0.25	ns, Min
T_{CINCK}/T_{CKCIN}	CIN input to CLK on A – D flip-flops	0.38 0.18	0.38 0.22	0.47 0.35	0.82 0.45	ns, Min
Set/Reset						
T_{RPW}	SR input minimum pulse width			0.30		ns, Min
T_{RQ}	Delay from SR input to AQ – DQ flip-flops	1.81	1.81	2.50	3.05	ns, Max
T_{CEO}	Delay from CE input to AQ – DQ flip-flops	0.75	0.65	0.92	1.36	ns, Max
F_{TOG}	Toggle frequency (for export control)			667		MHz

CLB Distributed RAM Switching Characteristics (SLICEM Only)

Table 39: **CLB Distributed RAM Switching Characteristics (SLICEM Only)**

Symbol	Description	Speed Grade				Units
		-4	-3	-2	-1L	
Sequential Delays						
T_{SHCKO}	Clock to A – D outputs	1.37	1.45	1.93	2.56	ns, Max
Setup and Hold Times Before/After Clock CLK						
T_{DS}/T_{DH}	AX – DX or AI – DI inputs to CLK	0.59 0.17	0.73 0.22	1.04 0.37	1.16 0.28	ns, Min
T_{AS}/T_{AH}	Address An inputs to clock	0.73 0.35	0.73 0.42	1.05 0.67	1.48 0.62	ns, Min
T_{WS}/T_{WH}	WE input to clock	0.31 –0.07	0.37 –0.07	0.59 –0.07	0.59 –0.17	ns, Min
T_{CECK}/T_{CKCE}	CE input to CLK	0.31 –0.07	0.37 –0.07	0.59 –0.07	0.59 –0.17	ns, Min

CLB Shift Register Switching Characteristics (SLICEM Only)

Table 40: **CLB Shift Register Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-4	-3	-2	-1L	
Sequential Delays						
T_{REG}	Clock to A – D outputs	1.56	1.91	2.27	2.89	ns, Max
Setup and Hold Times Before/After Clock CLK						
T_{WS}/T_{WH}	WE input to CLK	0.31 –0.07	0.37 –0.07	0.59 –0.07	0.59 –0.17	ns, Min
T_{CECK}/T_{CKCE}	CE input to CLK	0.31 –0.07	0.37 –0.07	0.59 –0.07	0.59 –0.17	ns, Min
T_{DS}/T_{DH}	AX – DX or AI – DI inputs to CLK	0.59 0.17	0.73 0.22	1.04 0.37	1.16 0.28	ns, Min

Block RAM Switching Characteristics

Table 41: **Block RAM Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-4	-3	-2	-1L	
Block RAM Clock to Out Delays						
T_{RCKO_DO}	Clock CLK to DOUT output (without output register)(1)	1.85	2.10	2.90	3.50	ns, Max
$T_{RCKO\_DO\_REG}$	Clock CLK to DOUT output (with output register)(2)	1.60	1.75	1.90	2.30	ns, Max
Setup and Hold Times Before/After Clock CLK						
$T_{RCCK\_ADDR}/T_{RCKC\_ADDR}$	ADDR inputs(3)	0.35 0.10	0.40 0.12	0.40 0.15	0.50 0.15	ns, Min
T_{RDCK_DI}/T_{RCKD_DI}	DIN inputs(4)	0.30 0.10	0.30 0.10	0.30 0.12	0.40 0.15	ns, Min
T_{RCCK_EN}/T_{RCKC_EN}	Block RAM Enable (EN) input	0.21 0.05	0.22 0.06	0.28 0.10	0.26 0.10	ns, Min
$T_{RCCK\_REGCE}/T_{RCKC\_REGCE}$	CE input of output register	0.20 0.10	0.20 0.10	0.25 0.12	0.28 0.15	ns, Min
T_{RCCK_WE}/T_{RCKC_WE}	Write Enable (WE) input	0.25 0.10	0.33 0.10	0.46 0.12	0.28 0.15	ns, Min
Maximum Frequency						
F_{MAX}	Block RAM in all modes	320	280	260	150	MHz

Notes:

1. T_{RCKO_DO} includes T_{RCKO_DOA} and T_{RCKO_DOPA} as well as the B port equivalent timing parameters.
2. $T_{RCKO\_DO\_REG}$ includes $T_{RCKO\_DOA\_REG}$ and $T_{RCKO\_DOPA\_REG}$ as well as the B port equivalent timing parameters.
3. The ADDR setup and hold must be met when EN is asserted (even when WE is deasserted). Otherwise, block RAM data corruption is possible.
4. T_{RDCK_DI} includes both A and B inputs as well as the parity inputs of A and B.

DSP48A1 Switching Characteristics

Table 42: **DSP48A1 Switching Characteristics**

Symbol	Description	Pre-adder	Multiplier	Post-adder	Speed Grade				Units
					-4	-3	-2	-1L	
Setup and Hold Times of Data/Control Pins to the Input Register Clock									
$T_{DSPDCK\_A\_A1REG}$/ $T_{DSPCKD\_A\_A1REG}$	A input to A1 register CLK	N/A	N/A	N/A	0.15 0.09	0.17 0.09	0.23 0.09	0.32 0.09	ns
$T_{DSPDCK\_D\_B1REG}$/ $T_{DSPCKD\_D\_B1REG}$	D input to B1 register CLK	Yes	N/A	N/A	1.23 –0.07	1.77 –0.07	1.99 –0.07	2.82 –0.07	ns
$T_{DSPDCK\_C\_CREG}$/ $T_{DSPCKD\_C\_CREG}$	C input to C register CLK	N/A	N/A	N/A	0.11 0.15	0.13 0.15	0.17 0.15	0.24 0.09	ns
$T_{DSPDCK\_D\_DREG}$/ $T_{DSPCKD\_D\_DREG}$	D input to D register CLK	N/A	N/A	N/A	0.09 0.15	0.10 0.15	0.14 0.15	0.19 0.12	ns
$T_{DSPDCK\_OPMODE\_B1REG}$/ $T_{DSPCKD\_OPMODE\_B1REG}$	OPMODE input to B1 register CLK	Yes	N/A	N/A	1.25 0.01	1.73 0.01	2.01 0.01	2.85 0.01	ns
$T_{DSPDCK\_OPMODE\_OPMODEREG}$/ $T_{DSPCKD\_OPMODE\_OPMODEREG}$	OPMODE input to OPMODE register CLK	N/A	N/A	N/A	0.18 0.26	0.21 0.26	0.28 0.26	0.40 0.12	ns
Setup and Hold Times of Data Pins to the Pipeline Register Clock									
$T_{DSPDCK\_A\_MREG}$/ $T_{DSPCKD\_A\_MREG}$	A input to M register CLK	N/A	Yes	N/A	1.88 –0.40	2.15 –0.40	3.71 –0.40	3.97 –0.40	ns
$T_{DSPDCK\_B\_MREG}$/ $T_{DSPCKD\_B\_MREG}$	B input to M register CLK	Yes	Yes	N/A	3.06 –0.68	3.69 –0.68	5.28 –0.68	7.00 –0.68	ns
$T_{DSPDCK\_D\_MREG}$/ $T_{DSPCKD\_D\_MREG}$	D input to M register CLK	Yes	Yes	N/A	3.00 –0.56	3.72 –0.56	4.82 –0.56	6.84 –0.56	ns
$T_{DSPDCK\_OPMODE\_MREG}$/ $T_{DSPCKD\_OPMODE\_MREG}$	OPMODE to M register CLK	Yes	Yes	N/A	3.01 –0.48	3.68 –0.48	4.85 –0.48	6.88 –0.48	ns
		No	Yes	N/A	1.88 –0.48	2.03 –0.48	3.02 –0.48	4.28 –0.48	ns
Setup and Hold Times of Data/Control Pins to the Output Register Clock									
$T_{DSPDCK\_A\_PREG}$/ $T_{DSPCKD\_A\_PREG}$	A input to P register CLK	N/A	Yes	Yes	3.43 –0.76	3.64 –0.76	5.38 –0.76	7.52 –0.76	ns
$T_{DSPDCK\_B\_PREG}$/ $T_{DSPCKD\_B\_PREG}$	B input to P register CLK	Yes	Yes	Yes	4.62 –0.59	5.47 –0.59	7.87 –0.59	10.55 –0.59	ns
		No	Yes	Yes	3.56 –0.93	3.82 –0.93	6.16 –0.93	8.12 –0.93	ns
$T_{DSPDCK\_C\_PREG}$/ $T_{DSPCKD\_C\_PREG}$	C input to P register CLK	N/A	N/A	Yes	1.43 –0.23	1.61 –0.23	2.30 –0.23	3.27 –0.23	ns
$T_{DSPDCK\_D\_PREG}$/ $T_{DSPCKD\_D\_PREG}$	D input to P register CLK	Yes	Yes	Yes	4.55 –0.92	5.50 –0.92	7.32 –0.92	10.39 –0.92	ns
$T_{DSPDCK\_OPMODE\_PREG}$/ $T_{DSPCKD\_OPMODE\_PREG}$	OPMODE input to P register CLK	Yes	Yes	Yes	4.56 –0.84	5.46 –0.84	7.35 –0.84	10.43 –0.84	ns
		No	Yes	Yes	1.59 –0.87	1.98 –0.87	2.55 –0.87	3.62 –0.87	ns
		No	No	Yes	1.66 –0.22	1.73 –0.22	2.67 –0.22	3.79 –0.22	ns

Table 42: **DSP48A1 Switching Characteristics *(Cont'd)***

Symbol	Description	Pre-adder	Multiplier	Post-adder	Speed Grade				Units
					-4	-3	-2	-1L	
Clock to Out from Output Register Clock to Output Pin									
$T_{DSPCKO\_P\_PREG}$	CLK (PREG) to P output	N/A	N/A	N/A	0.83	1.02	1.34	1.90	ns
Clock to Out from Pipeline Register Clock to Output Pins									
$T_{DSPCKO\_P\_MREG}$	CLK (MREG) to P output	N/A	N/A	Yes	2.55	2.98	4.19	5.83	ns
Clock to Out from Input Register Clock to Output Pins									
$T_{DSPCKO\_P\_A1REG}$	CLK (A1REG) to P output	N/A	Yes	Yes	4.23	4.78	6.80	9.65	ns
$T_{DSPCKO\_P\_B1REG}$	CLK (B1REG) to P output	N/A	Yes	Yes	4.21	4.68	6.79	9.63	ns
$T_{DSPCKO\_P\_CREG}$	CLK (CREG) to P output	N/A	N/A	Yes	2.30	2.70	3.70	5.24	ns
$T_{DSPCKO\_P\_DREG}$	CLK (DREG) to P output	Yes	Yes	Yes	5.48	6.62	9.06	12.53	ns
Combinatorial Delays from Input Pins to Output Pins									
$T_{DSPDO\_A\_P}$	A input to P output	N/A	No	Yes	2.21	2.53	3.41	4.73	ns
		N/A	Yes	No	3.09	3.54	4.83	6.74	ns
		N/A	Yes	Yes	4.05	4.36	6.38	8.94	ns
$T_{DSPDO\_B\_P}$	B input to P output	Yes	No	No	2.43	3.53	3.91	5.55	ns
		Yes	Yes	No	4.27	5.36	6.88	9.76	ns
		Yes	Yes	Yes	5.24	6.18	8.43	11.96	ns
$T_{DSPDO\_C\_P}$	C input to P output	N/A	N/A	Yes	2.05	2.33	3.30	4.68	ns
$T_{DSPDO\_D\_P}$	D input to P output	Yes	Yes	Yes	5.17	6.21	8.32	11.81	ns
$T_{DSPDO\_OPMODE\_P}$	OPMODE input to P output	Yes	Yes	Yes	5.18	6.17	8.35	11.84	ns
		No	Yes	Yes	4.05	4.52	6.52	9.25	ns
		No	No	Yes	2.21	2.69	3.55	5.03	ns
Maximum Frequency									
F_{MAX}	All registers used	Yes	Yes	Yes	320	287	250	150	MHz

Notes:
1. A Yes signifies that the component is in the path. A No signifies that the component is being bypassed. N/A signifies not applicable because no path exists.

Table 43: **Device DNA Interface Port Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-4	-3	-2	-1L	
T_{DNASSU}	Setup time on SHIFT before the rising edge of CLK	7				ns, Min
T_{DNASH}	Hold time on SHIFT after the rising edge of CLK	1				ns, Min
T_{DNADSU}	Setup time on DIN before the rising edge of CLK	7				ns, Min
T_{DNADH}	Hold time on DIN after the rising edge of CLK	1				ns, Min
T_{DNARSU}	Setup time on READ before the rising edge of CLK	7				ns, Min
		1,000				ns, Max
T_{DNARH}	Hold time on READ after the rising edge of CLK	1				ns, Min
$T_{DNADCKO}$	Clock-to-output delay on DOUT after rising edge of CLK	0.5				ns, Min
		6				ns, Max
$T_{DNACLKF}$(2)	CLK frequency	2				MHz, Max
$T_{DNACLKL}$	CLK Low time	50				ns, Min
$T_{DNACLKH}$	CLK High time	50				ns, Min

Notes:
1. The minimum READ pulse width is 8 ns, the maximum READ pulse width is 1 µs.
2. Also applies to TCK when reading DNA through the boundary-scan port.

Table 44: **Suspend Mode Switching Characteristics**

Symbol	Description	Min	Max	Units
Entering Suspend Mode				
$T_{SUSPENDHIGH\_AWAKE}$	Rising edge of SUSPEND pin to falling edge of AWAKE pin without glitch filter	2.5	14	ns
$T_{SUSPENDFILTER}$	Adjustment to SUSPEND pin rising edge parameters when glitch filter enabled	31	430	ns
$T_{SUSPEND\_GWE}$	Rising edge of SUSPEND pin until FPGA output pins drive their defined SUSPEND constraint behavior (without glitch filter)	–	15	ns
$T_{SUSPEND\_GTS}$	Rising edge of SUSPEND pin to write-protect lock on all writable clocked elements (without glitch filter)	–	15	ns
$T_{SUSPEND\_DISABLE}$	Rising edge of the SUSPEND pin to FPGA input pins and interconnect disabled (without glitch filter)	–	1500	ns
Exiting Suspend Mode				
$T_{SUSPENDLOW\_AWAKE}$	Falling edge of the SUSPEND pin to rising edge of the AWAKE pin. Does not include DCM or PLL lock time.	7	75	µs
$T_{SUSPEND\_ENABLE}$	Falling edge of the SUSPEND pin to FPGA input pins and interconnect re-enabled	7	41	µs
T_{AWAKE_GWE1}	Rising edge of the AWAKE pin until write-protect lock released on all writable clocked elements, using **sw_clk:InternalClock** and **sw_gwe_cycle:1**.	–	80	ns
T_{AWAKE_GWE512}	Rising edge of the AWAKE pin until write-protect lock released on all writable clocked elements, using **sw_clk:InternalClock** and **sw_gwe_cycle:512**.	–	20.5	µs
T_{AWAKE_GTS1}	Rising edge of the AWAKE pin until outputs return to the behavior described in the FPGA application, using **sw_clk:InternalClock** and **sw_gts_cycle:1**.	–	80	ns
T_{AWAKE_GTS512}	Rising edge of the AWAKE pin until outputs return to the behavior described in the FPGA application, using **sw_clk:InternalClock** and **sw_gts_cycle:512**.	–	20.5	µs
T_{SCP_AWAKE}	Rising edge of SCP pins to rising edge of AWAKE pin	7	75	µs

Configuration Switching Characteristics

Table 45: **Configuration Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-4	-3	-2	-1L	
Power-up Timing Characteristics						
T_{PL}(2)	PROGRAM_B Latency	4	4	4		ms, Max
T_{POR}(2)	Power-on-Reset	50	50	50		ms, Max
$T_{PROGRAM}$	PROGRAM_B Pulse Width	500	500	500		ns, Min
Slave Serial Mode Programming Switching						
T_{DCCK}/T_{CCKD}	DIN Setup/Hold, slave mode	6.0/1.0	6.0/1.0	6.0/1.0		ns, Min
T_{CCO}	CCLK to DOUT	12	12	12		ns, Max
F_{SCCK}	Slave mode external CCLK	80	80	80		MHz, Max
Slave SelectMAP Mode Programming Switching						
T_{SMDCCK}/T_{SMCCKD}	SelectMAP Data Setup/Hold	6.0/1.0	6.0/1.0	6.0/1.0		ns, Min
$T_{SMCSCCK}/T_{SMCCKCS}$	CSI_B Setup/Hold	7.0/0.0	7.0/0.0	7.0/0.0		ns, Min
T_{SMCCKW}/T_{SMWCCK}	RDWR_B Setup/Hold	17.0/1.0	17.0/1.0	17.0/1.0		ns, Min
$T_{SMCKCSO}$	CSO_B clock to out	16	16	16		ns, Min
T_{SMCO}	CCLK to DATA out in readback	13	13	13	N/A	ns, Max
T_{SMCKBY}	CCLK to BUSY out in readback	12	12	12	N/A	ns, Max
F_{SMCCK}	Maximum CCLK frequency	50	50	50		MHz, Max
F_{RBCCK}	Maximum Readback CCLK frequency	20	20	20	N/A	MHz, Max
Boundary-Scan Port Timing Specifications						
T_{TAPTCK}	TMS and TDI Setup time before TCK	10	10	10		ns, Min
T_{TCKTAP}	TMS and TDI Hold time after TCK	5.5	5.5	5.5		ns, Min
T_{TCKTDO}	TCK falling edge to TDO output valid	6.5	6.5	6.5		ns, Max
T_{TCKH}	TCK clock minimum High time	12	12	12		ns, Min
T_{TCKL}	TCK clock minimum Low time	12	12	12		ns, Min
F_{TCK}	Maximum configuration TCK clock frequency	33	33	33		MHz, Max
F_{TCKB}	Maximum boundary-scan TCK clock frequency	33	33	33		MHz, Max
F_{TCKAES}	Maximum AES key TCK clock frequency	2	2	2		MHz, Max
BPI Master Flash Mode Programming Switching						
T_{BPICCO}(3)	A[25:0], FCS_B, FOE_B, FWE_B, LDC outputs valid after CCLK falling edge	15	15	15		ns, Min
T_{BPIDCC}/T_{BPICCD}	Setup/Hold on D[15:0] data input pins	5.0/1.0	5.0/1.0	5.0/1.0		ns, Min
SPI Master Flash Mode Programming Switching						
$T_{SPIDCC}/T_{SPIDCCD}$	DIN, MISO0, MISO1, MISO2, MISO3, Setup/Hold before/after the rising CCLK edge	5.0/1.0	5.0/1.0	5.0/1.0		ns, Min
T_{SPICCM}	MOSI clock to out	13	13	13		ns, Max
$T_{SPICCFC}$	CSO_B clock to out	16	16	16		ns, Max

Table 45: **Configuration Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade				Units
		-4	-3	-2	-1L	
CCLK Output (Master Modes)						
T_{MCCKL}	Master CCLK clock duty cycle Low	40/60				%, Min/Max
T_{MCCKH}	Master CCLK clock duty cycle High	40/60				%, Min/Max
F_{MCCK}	Maximum Frequency, master mode	40	40	40		MHz, Max
$F_{MCCKTOL}$	Frequency Tolerance, master mode	±50	±50	±50		%
CCLK Input (Slave Modes)						
T_{SCCKL}	Slave CCLK clock minimum Low time	5	5	5		ns, Min
T_{SCCKH}	Slave CCLK clock minimum High time	5	5	5		ns, Min
USERCCLK Input						
$T_{USERCCLKL}$	USERCCLK clock minimum Low time	12	12	12		ns, Min
$T_{USERCCLKH}$	USERCCLK clock minimum High time	12	12	12		ns, Min
$F_{USERCCLK}$	Maximum USERCCLK frequency	40	40	40		MHz, Max

Notes:

1. Maximum frequency and setup/hold timing parameters are for 3.3V and 2.5V configuration voltages.
2. To support longer delays in configuration, use the design solutions described in the *Spartan-6 FPGA Configuration User Guide*
3. Only during configuration, the last edge is determined by a weak pull-up/pull-down resistor in the I/O.

Clock Buffers and Networks

Table 46: **Global Clock Switching Characteristics**

Symbol	Description	Devices	Speed Grade				Units
			-4	-3	-2	-1L	
T_{GSI}	S pin Setup to I0/I1 inputs	LX Family	N/A	0.31	0.48	0.60	ns
		LXT Family	0.25	0.31	0.48	N/A	ns
T_{GIO}	BUFGMUX delay from I0/I1 to O	XC6SLX4	N/A				ns
		XC6SLX9	N/A				ns
		XC6SLX16	N/A		0.42		ns
		XC6SLX25	N/A				ns
		XC6SLX25T				N/A	ns
		XC6SLX45	N/A		0.42		ns
		XC6SLX45T			0.42	N/A	ns
		XC6SLX75	N/A				ns
		XC6SLX75T				N/A	ns
		XC6SLX100	N/A				ns
		XC6SLX100T				N/A	ns
		XC6SLX150	N/A				ns
		XC6SLX150T				N/A	ns
Maximum Frequency							
F_{MAX}	Global clock tree (BUFG)	LX Family	N/A	400	375		MHz
		LXT Family	400	400	375	N/A	MHz

Table 47: **Input/Output Clock Switching Characteristics (BUFIO2)**

Symbol	Description	Devices	Speed Grade				Units
			-4	-3	-2	-1L	
T_{BUFCKO_O}	Clock to out delay from I to O	LX Family	N/A	0.82	1.09	1.80	ns
		LXT Family	0.67	0.82	1.09	N/A	ns
Maximum Frequency							
F_{MAX}	I/O clock tree (BUFIO2)	LX Family	N/A	525	500		MHz
		LXT Family	540	525	500	N/A	MHz

Table 48: **Input/Output Clock Switching Characteristics (BUFPLL)**

Symbol	Description	Devices	Speed Grade				Units
			-4	-3	-2	-1L	
Maximum Frequency							
F_{MAX}	BUFPLL clock tree (BUFPLL)	LX Family	N/A	1050	950		MHz
		LXT Family	1080	1050	950	N/A	MHz

PLL Switching Characteristics

Table 49: **PLL Specification**

Symbol	Description	Device[1]	Speed Grade				Units
			-4	-3	-2	-1L	
F_{INMAX}	Maximum Input Clock Frequency from I/O Clock	LX Family	N/A	525	450		MHz
		LXT Family	540	525	450	N/A	MHz
	Maximum Input Clock Frequency from Global Clock	LX Family	N/A	400	375		MHz
		LXT Family		400	375	N/A	MHz
F_{INMIN}	Minimum Input Clock Frequency	LX Family	N/A	19	19		MHz
		LXT Family	19	19	19	N/A	MHz
$F_{INJITTER}$	Maximum Input Clock Period Jitter	All	<20% of clock input period or 1 ns Max				
F_{INDUTY}	Allowable Input Duty Cycle: 19—199 MHz	All	25/75				%
	Allowable Input Duty Cycle: 200—299 MHz	All	35/65				%
	Allowable Input Duty Cycle: > 300 MHz	All	45/55				%
F_{VCOMIN}	Minimum PLL VCO Frequency	LX Family	N/A	400	400	400	MHz
		LXT Family	400	400	400	N/A	MHz
F_{VCOMAX}	Maximum PLL VCO Frequency	LX Family	N/A	1050	1000	1000	MHz
		LXT Family	1080	1050	1000	N/A	MHz
$F_{BANDWIDTH}$	Low PLL Bandwidth at Typical[3]	All	1	1	1	1	MHz
	High PLL Bandwidth at Typical[3]	All	4	4	4	4	MHz
$T_{STAPHAOFFSET}$	Static Phase Offset of the PLL Outputs	All	0.12	0.12	0.12		ns
$T_{OUTJITTER}$	PLL Output Jitter[3]	All	Note 2				
$T_{OUTDUTY}$	PLL Output Clock Duty Cycle Precision[4]	All	0.15	0.15	0.20		ns
$T_{LOCKMAX}$	PLL Maximum Lock Time	All	100	100	100	100	µs
F_{OUTMAX}	PLL Maximum Output Frequency for BUFGMUX	LX Family	N/A	400	375		MHz
		LXT Family	400	400	375	N/A	MHz
F_{OUTMAX}	PLL Maximum Output Frequency for BUFPLL	LX Family	N/A	1050	950		MHz
		LXT Family	1080	1050	950	N/A	MHz
F_{OUTMIN}	PLL Minimum Output Frequency[5]	All	3.125	3.125	3.125	3.125	MHz
$T_{EXTFDVAR}$	External Clock Feedback Variation	All	< 20% of clock input period or 1 ns Max				
$RST_{MINPULSE}$	Minimum Reset Pulse Width	All	5	5	5	5	ns
F_{PFDMAX}[5]	Maximum Frequency at the Phase Frequency Detector	LX Family	N/A	500	400		MHz
		LXT Family	500	500	400	N/A	MHz
F_{PFDMIN}	Minimum Frequency at the Phase Frequency Detector	LX Family	N/A	19	19		MHz
		LXT Family	19	19	19	N/A	MHz
$T_{FBDELAY}$	Maximum Delay in the Feedback Path	All	3 ns Max or one CLKIN cycle				

Notes:
1. LX devices are not available with a -4 speed grade; LXT devices are not available with a -1L speed grade.
2. Values for this parameter are available in the Clocking Wizard.
3. The PLL does not filter typical spread spectrum input clocks because they are usually far below the bandwidth filter frequencies.
4. Includes global clock buffer.
5. Calculated as $F_{VCO}/128$ assuming output duty cycle is 50%.
6. When using CLK_FEEDBACK = CLKOUT0 with BUFIO2 feedback, the feedback frequency will be higher than the phase frequency detector frequency. $F_{PFDMAX} = F_{CLKFB}$ / CLKFBOUT_MULT

DCM Switching Characteristics

Table 50: **Operating Frequency Ranges and Conditions for the Delay-Locked Loop (DLL)(1)**

Symbol	Description	Speed Grade								Units
		-4		-3		-2		-1L		
		Min	Max	Min	Max	Min	Max	Min	Max	
Input Frequency Ranges										
CLKIN_FREQ_DLL	Frequency of the CLKIN clock input. Also described as F_{CLKIN}.	5(2)	280(3)	5(2)	280(3)	5(2)	250(3)	5(2)	175(3)	MHz
Input Pulse Requirements										
CLKIN_PULSE	CLKIN pulse width as a percentage of the CLKIN period for CLKIN_FREQ_DLL < 150 MHz	40	60	40	60	40	60	40	60	%
	CLKIN pulse width as a percentage of the CLKIN period for CLKIN_FREQ_DLL > 150 MHz	45	55	45	55	45	55	45	55	%
Input Clock Jitter Tolerance and Delay Path Variation(4)										
CLKIN_CYC_JITT_DLL_LF	Cycle-to-cycle jitter at the CLKIN input for CLKIN_FREQ_DLL < 150 MHz	–	±300	–	±300	–	±300	–	±300	ps
CLKIN_CYC_JITT_DLL_HF	Cycle-to-cycle jitter at the CLKIN input for CLKIN_FREQ_DLL > 150 MHz.	–	±150	–	±150	–	±150	–	±150	ps
CLKIN_PER_JITT_DLL	Period jitter at the CLKIN input.	–	±1	–	±1	–	±1	–	±1	ns
CLKFB_DELAY_VAR_EXT	Allowable variation of the off-chip feedback delay from the DCM output to the CLKFB input.	–	±1	–	±1	–	±1	–	±1	ns

Notes:
1. DLL specifications apply when using any of the DLL outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, or CLKDV.
2. When operating independently of the DLL, the DFS supports lower CLKIN_FREQ_DLL frequencies. See Table 52.
3. The CLKIN_DIVIDE_BY_2 attribute can be used to increase the effective input frequency range up to the F_{MAX} for the global clock BUFG, see Table 46. When set to TRUE, the CLKIN_DIVIDE_BY_2 attribute divides the incoming clock frequency by two as it enters the DCM.
4. CLKIN_FREQ_DLL input jitter beyond these limits can cause the DCM to lose LOCK, indicated by the LOCKED output deasserting. The user must then reset the DCM.
5. When using both DCMs in a CMT, both DCMs must be LOCKED.

Table 51: **Switching Characteristics for the Delay-Locked Loop (DLL) (1)**

Symbol	Description	Speed Grade								Units
		-4		-3		-2		-1L		
		Min	Max	Min	Max	Min	Max	Min	Max	
Output Frequency Ranges										
CLKOUT_FREQ_CLK0	Frequency for the CLK0 and CLK180 outputs.	5	280	5	280	5	250			MHz
CLKOUT_FREQ_CLK90	Frequency for the CLK90 and CLK270 outputs.	5	200	5	200	5	200			MHz
CLKOUT_FREQ_2X	Frequency for the CLK2X and CLK2X180 outputs.	10	375	10	375	10	334			MHz
CLKOUT_FREQ_DV	Frequency for the CLKDV output.	0.3125	186	0.3125	186	0.3125	166			MHz
Output Clock Jitter(2,3,4)										
CLKOUT_PER_JITT_0	Period jitter at the CLK0 output.	–	±100	–	±100	–	±100	–		ps
CLKOUT_PER_JITT_90	Period jitter at the CLK90 output.	–	±150	–	±150	–	±150	–		ps
CLKOUT_PER_JITT_180	Period jitter at the CLK180 output.	–	±150	–	±150	–	±150	–		ps
CLKOUT_PER_JITT_270	Period jitter at the CLK270 output.	–	±150	–	±150	–	±150	–		ps
CLKOUT_PER_JITT_2X	Period jitter at the CLK2X and CLK2X180 outputs.	Maximum = ±[0.5% of CLKIN period + 100]								ps
CLKOUT_PER_JITT_DV1	Period jitter at the CLKDV output when performing integer division.	–	±150	–	±150	–	±150	–	±150	ps
CLKOUT_PER_JITT_DV2	Period jitter at the CLKDV output when performing non-integer division.	Maximum = ±[0.5% of CLKIN period + 100]								ps
Duty Cycle(4)										
CLKOUT_DUTY_CYCLE_DLL	Duty cycle variation for the CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV outputs, including the BUFGMUX and clock tree duty-cycle distortion.	Typical = ±[1% of CLKIN period + 350]								ps
Phase Alignment(4)										
CLKIN_CLKFB_PHASE	Phase offset between the CLKIN and CLKFB inputs.	–	±150	–	±150	–	±150	–	±150	ps
CLKOUT_PHASE_DLL	Phase offset between DLL outputs for CLK0 to CLK2X (not CLK2X180).	Maximum = ±[1% of CLKIN period + 100]								ps
	Phase offset between DLL outputs for all others.									ps
LOCK_DLL(3)	When using the DLL alone: The time from deassertion at the DCM's reset input to the rising transition at its LOCKED output. When the DCM is locked, the CLKIN and CLKFB signals are in phase. 5 MHz < CLKIN_FREQ_DLL < 50 MHz.	–	5	–	5	–	5	–	5	ms
	When using the DLL alone: The time from deassertion at the DCM's reset input to the rising transition at its LOCKED output. When the DCM is locked, the CLKIN and CLKFB signals are in phase. CLKIN_FREQ_DLL > 50 MHz	–	0.60	–	0.60	–	0.60	–	0.60	ms

Table 51: **Switching Characteristics for the Delay-Locked Loop (DLL) (1) *(Cont'd)***

Symbol	Description	Speed Grade								Units
		-4		-3		-2		-1L		
		Min	Max	Min	Max	Min	Max	Min	Max	
Delay Lines										
DCM_DELAY_STEP(5)	Finest delay resolution, averaged over all steps.	10	40	10	40	10	40	10	40	ps

Notes:
1. The values in this table are based on the operating conditions described in Table 2 and Table 50.
2. Indicates the maximum amount of output jitter that the DCM adds to the jitter on the CLKIN input.
3. For optimal jitter tolerance and faster LOCK time, use the CLKIN_PERIOD attribute.
4. Some jitter and duty-cycle specifications include 1% of input clock period or 0.01 UI. For example, this data sheet specifies a maximum jitter of ±(1% of CLKIN period + 150 ps). Assuming that the CLKIN frequency is 100 MHz, the equivalent CLKIN period is 10 ns. Since 1% of 10 ns is 0.1 ns or 100 ps, the maximum jitter is ±(100 ps + 150 ps) = ±250 ps.
5. A typical delay step size is 23 ps.

Table 52: **Recommended Operating Conditions for the Digital Frequency Synthesizer (DFS) (1)**

Symbol	Description	Speed Grade								Units
		-4		-3		-2		-1L		
		Min	Max	Min	Max	Min	Max	Min	Max	
Input Frequency Ranges(2)										
CLKIN_FREQ_FX	Frequency for the CLKIN input. Also described as F_{CLKIN}.	0.5	375	0.5	375	0.5	333			MHz
Input Clock Jitter Tolerance(3)										
CLKIN_CYC_JITT_FX_LF	Cycle-to-cycle jitter at the CLKIN input, based on CLKFX output frequency: FCLKFX < 150 MHz.	–	±300	–	±300	–	±300	–	±300	ps
CLKIN_CYC_JITT_FX_HF	Cycle-to-cycle jitter at the CLKIN input, based on CLKFX output frequency: FCLKFX > 150 MHz.	–	±150	–	±150	–	±150	–	±150	ps
CLKIN_PER_JITT_FX	Period jitter at the CLKIN input.	–	±1	–	±1	–	±1	–	±1	ns

Notes:
1. DFS specifications apply when using either of the DFS outputs (CLKFX or CLKFX180).
2. When using both DFS and DLL outputs on the same DCM, follow the more restrictive CLKIN_FREQ_DLL specifications in Table 50.
3. CLKIN input jitter beyond these limits can cause the DCM to lose LOCK.

Table 53: **Switching Characteristics for the Digital Frequency Synthesizer (DFS) for DCM_SP (1)**

Symbol	Description	Speed Grade								Units
		-4		-3		-2		-1L		
		Min	Max	Min	Max	Min	Max	Min	Max	
Output Frequency Ranges										
CLKOUT_FREQ_FX	Frequency for the CLKFX and CLKFX180 outputs	5	375	5	375	5	333			MHz
Output Clock Jitter(2,3)										
CLKOUT_PER_JITT_FX	Period jitter at the CLKFX and CLKFX180 outputs. When CLKIN < 20 MHz	Use the Clocking Wizard								ps
	Period jitter at the CLKFX and CLKFX180 outputs. When CLKIN > 20 MHz	Typical = ±(1% of CLKFX period + 100)								ps
Duty Cycle(4,5)										
CLKOUT_DUTY_CYCLE_FX	Duty cycle precision for the CLKFX and CLKFX180 outputs including the BUFGMUX and clock tree duty-cycle distortion	Maximum = ±(1% of CLKFX period + 350)								ps
Phase Alignment(5)										
CLKOUT_PHASE_FX	Phase offset between the DFS CLKFX output and the DLL CLK0 output when both the DFS and DLL are used	–	±200	–	±200	–	±200	–	±200	ps
CLKOUT_PHASE_FX180	Phase offset between the DFS CLKFX180 output and the DLL CLK0 output when both the DFS and DLL are used	Maximum = ±(1% of CLKFX period + 200)								ps
LOCKED Time										
LOCK_FX(2)	When 5 MHz < FCLKIN < 50 MHz, the time from deassertion at the DCM's reset input to the rising transition at its LOCKED output. The DFS asserts LOCKED when the CLKFX and CLKFX180 signals are valid. When using both the DLL and the DFS, use the longer locking time.	–	5	–	5	–	5	–	5	ms
	When FCLKIN > 50 MHz, the time from deassertion at the DCM's reset input to the rising transition at its LOCKED output. The DFS asserts LOCKED when the CLKFX and CLKFX180 signals are valid. When using both the DLL and the DFS, use the longer locking time.	–	0.45	–	0.45	–	0.45	–	0.45	ms

Notes:
1. The values in this table are based on the operating conditions described in Table 2 and Table 52.
2. For optimal jitter tolerance and a faster LOCK time, use the CLKIN_PERIOD attribute.
3. Output jitter is characterized using a reasonable noise environment (40 SSOs and 25% CLB switching). Output jitter strongly depends on the environment, including the number of SSOs, the output drive strength, CLB utilization, CLB switching activities, switching frequency, power supply, and PCB design. The actual maximum output jitter depends on the system application.
4. The CLKFX, CLKFXDV, and CLKFX180 outputs have a duty cycle of approximately 50%.
5. Some duty cycle and alignment specifications include a percentage of the CLKFX output period. For example, this data sheet specifies a maximum CLKFX jitter of ±(1% of CLKFX period + 200 ps). Assuming that the CLKFX output frequency is 100 MHz, the equivalent CLKFX period is 10 ns, and 1% of 10 ns is 0.1 ns or 100 ps. Accordingly, the maximum jitter is ±(100 ps + 200 ps) = ±300 ps.

Table 54: **Switching Characteristics for the Digital Frequency Synthesizer DFS (DCM_CLKGEN) (1)**

Symbol	Description	Speed Grade								Units
		-4		-3		-2		-1L		
		Min	Max	Min	Max	Min	Max	Min	Max	
Output Frequency Ranges (DCM_CLKGEN)										
CLKOUT_FREQ_FX	Frequency for the CLKFX and CLKFX180 outputs	5	375	5	375	5	333	5	200	MHz
CLKOUT_FREQ_FXDV	Frequency for the CLKFXDV output	0.15625	187.5	0.15625	187.5	0.15625	166.5	0.15625	100	MHz
Output Clock Jitter(2, 3)										
CLKOUT_PER_JITT_FX	Period jitter at the CLKFX and CLKFX180 outputs.	Typical = ±[0.2% of CLKFX period + 100]								ps
CLKOUT_PER_JITT_FXDV	Period jitter at the CLKFXDV output.	Typical = ±[0.2% of CLKFX period + 100]								ps
CLKFX_FREEZE_VAR	CLKFX period change in free running oscillator mode at the same temperature. FCLKFX > 50 MHz	Maximum = ±3% of CLKFX period								ps
	CLKFX period change in free running oscillator mode at the same temperature. FCLKFX < 50 MHz	Maximum = ±5% of CLKFX period								ps
CLKFX_FREEZE_TEMP_SLOPE	CLKFX period will change in free_oscillator mode over temperature. Add to CLKFX_FREEZE_VAR to determine total CLKFX period change. Percentage change for CLKFX period over 1°C.	Maximum = 0.1								%/°C
Duty Cycle (4, 5)										
CLKOUT_DUTY_CYCLE_FX	Duty cycle precision for the CLKFX and CLKFX180 outputs, including the BUFGMUX and clock tree duty-cycle distortion	Maximum = ±[1% of CLKFX period + 350]								ps
CLKOUT_DUTY_CYCLE_FXDV	Duty cycle precision for the CLKFXDV outputs, including the BUFGMUX and clock tree duty-cycle distortion	Maximum = ±[1% of CLKFX period + 350]								ps
Lock Time										
LOCK_FX(2)	The time from deassertion at the DCM's Reset input to the rising transition at its LOCKED output. The DFS asserts LOCKED when the CLKFX, CLKFX180, and CLKFXDV signals are valid. Lock time requires CLKFX_DIVIDE < F_{IN}/(0.50 MHz) when: 5 MHz < F_{CLKIN} < 50 MHz	–	50	–	50	–	50	–	50	ms
	when: F_{CLKIN} > 50 MHz	–	5	–	5	–	5	–	5	ms

Table 54: **Switching Characteristics for the Digital Frequency Synthesizer DFS (DCM_CLKGEN) (1) *(Cont'd)***

Symbol	Description	Speed Grade								Units
		-4		-3		-2		-1L		
		Min	Max	Min	Max	Min	Max	Min	Max	
Spread Spectrum										
$F_{CLKIN\_FIXED\_SPREAD\_SPECTRUM}$	Frequency of the CLKIN input for fixed spread spectrum (SPREAD_SPECTRUM = CENTER_LOW_SPREAD/ CENTER_HIGH_SPREAD)					30	200			MHz
$T_{CENTER\_LOW\_SPREAD}$ (6)	Spread at the CLKFX output for fixed spread spectrum (SPREAD_SPECTRUM = CENTER_LOW_SPREAD)					Typical = $\frac{100}{CLKFX\_DIVIDE}$ Maximum = 250				ps
$T_{CENTER\_HIGH\_SPREAD}$ (6)	Spread at the CLKFX output for fixed spread spectrum (SPREAD_SPECTRUM= CENTER_HIGH_SPREAD)					Typical = $\frac{240}{CLKFX\_DIVIDE}$ Maximum = 400				ps
$F_{MOD\_FIXED\_SPREAD\_SPECTRUM}$ (6)	Average modulation frequency when using fixed spread spectrum (SPREAD_SPECTRUM = CENTER_LOW_SPREAD / CENTER_HIGH_SPREAD)	Typical = $F_{IN}/1024$								MHz

Notes:
1. The values in this table are based on the operating conditions described in Table 2 and Table 52.
2. For optimal jitter tolerance and a faster LOCK time, use the CLKIN_PERIOD attribute.
3. Output jitter is characterized using a reasonable noise environment (40 SSOs and 25% CLB switching). Output jitter strongly depends on the environment, including the number of SSOs, the output drive strength, CLB utilization, CLB switching activities, switching frequency, power supply, and PCB design. The actual maximum output jitter depends on the system application.
4. The CLKFX, CLKFXDV, and CLKFX180 outputs have a duty cycle of approximately 50%.
5. Some duty-cycle and alignment specifications include a percentage of the CLKFX output period. For example, this data sheet specifies a maximum CLKFX jitter of ±(1% of CLKFX period + 200 ps). Assuming that the CLKFX output frequency is 100 MHz, the equivalent CLKFX period is 10 ns, and 1% of 10 ns is 0.1 ns or 100 ps. Accordingly, the maximum jitter is ±(100 ps + 200 ps) = ±300 ps.
6. When using CENTER_LOW_SPREAD, CENTER_HIGH_SPREAD, the valid values for CLKFX_MULTIPLY are limited to 2 through 32, and the valid values for CLKFX_DIVIDE limited to are limited to 1 through 4.

Table 55: **Recommended Operating Conditions for the Phase-Shift Clock in Variable Phase Mode**

Symbol	Description	Speed Grade								Units
		-4		-3		-2		-1L		
		Min	Max	Min	Max	Min	Max	Min	Max	
Operating Frequency Ranges										
PSCLK_FREQ	Frequency for the PSCLK input.	1	167	1	167	1	167	1	167	MHz
Input Pulse Requirements										
PSCLK_PULSE	PSCLK pulse width as a percentage of the PSCLK period.	40	60	40	60	40	60	40	60	%

Table 56: **Switching Characteristics for the Phase-Shift Clock in Variable Phase Mode (1)**

Symbol	Description	Amount of Phase Shift	Units
Phase Shifting Range			
MAX_STEPS(2)	When CLKIN < 60 MHz, the maximum allowed number of DCM_DELAY_STEP steps for a given CLKIN clock period, where T = CLKIN clock period in ns. When using CLKIN_DIVIDE_BY_2 = TRUE, double the clock-effective clock period.	±(INTEGER(10 x (TCLKIN – 3 ns)))	steps
	When CLKIN ≥ 60 MHz, the maximum allowed number of DCM_DELAY_STEP steps for a given CLKIN clock period, where T = CLKIN clock period in ns. When using CLKIN_DIVIDE_BY_2 = TRUE, double the clock-effective clock period.	±(INTEGER(15 x (TCLKIN – 3 ns)))	steps
FINE_SHIFT_RANGE_MIN	Minimum guaranteed delay for variable phase shifting.	±(MAX_STEPS x DCM_DELAY_STEP_MIN)	ns
FINE_SHIFT_RANGE_MAX	Maximum guaranteed delay for variable phase shifting	±(MAX_STEPS x DCM_DELAY_STEP_MAX)	ns

Notes:
1. The values in this table are based on the operating conditions described in Table 50 and Table 55.
2. The maximum variable phase shift range, MAX_STEPS, is only valid when the DCM has no initial fixed-phase shifting, that is, the PHASE_SHIFT attribute is set to 0.
3. The DCM_DELAY_STEP values are provided at the end of Table 51.

Table 57: **Miscellaneous DCM Timing Parameters(1)**

Symbol	Description	Min	Max	Units
DCM_RST_PW_MIN	Minimum duration of a RST pulse width	3	–	CLKIN cycles

Notes:
1. This limit only applies to applications that use the DCM DLL outputs (CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV). The DCM DFS outputs (CLKFX, CLKFXDV, CLKFX180) are unaffected.

Table 58: **Frequency Synthesis**

Attribute	Min	Max
CLKFX_MULTIPLY (DCM_SP)	2	32
CLKFX_DIVIDE (DCM_SP)	1	32
CLKDV_DIVIDE (DCM_SP)	1.5	16
CLKFX_MULTIPLY (DCM_CLKGEN)	2	256
CLKFX_DIVIDE (DCM_CLKGEN)	1	256
CLKFXDV_DIVIDE (DCM_CLKGEN)	2	32

Table 59: **DCM Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-4	-3	-2	-1L	
T_{DMCCK_PSEN}/ T_{DMCKC_PSEN}	PSEN Setup/Hold	1.50 0.00	1.50 0.00	1.50 0.00	1.50 0.00	ns
$T_{DMCCK\_PSINCDEC}$/ $T_{DMCKC\_PSINCDEC}$	PSINCDEC Setup/Hold	1.50 0.00	1.50 0.00	1.50 0.00	1.50 0.00	ns
T_{DMCKO_PSDONE}	Clock to out of PSDONE	1.50	1.50	1.50	1.50	ns

Spartan-6 Device Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. The representative values for typical pin locations and normal clock loading are listed in Table 60 through Table 66. Values are expressed in nanoseconds unless otherwise noted.

Table 60: **Global Clock Input to Output Delay Without DCM or PLL**

Symbol	Description	Device	Speed Grade				Units
			-4	-3	-2	-1L	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, *without* DCM or PLL							
T_{ICKOF}	Global Clock and OUTFF *without* DCM or PLL	XC6SLX4	N/A				ns
		XC6SLX9	N/A				ns
		XC6SLX16	N/A	6.42	7.48		ns
		XC6SLX25	N/A				ns
		XC6SLX25T				N/A	ns
		XC6SLX45	N/A	6.88	8.10		ns
		XC6SLX45T				N/A	ns
		XC6SLX75	N/A				ns
		XC6SLX75T				N/A	ns
		XC6SLX100	N/A				ns
		XC6SLX100T				N/A	ns
		XC6SLX150	N/A				ns
		XC6SLX150T				N/A	ns

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

Table 61: **Global Clock Input to Output Delay With DCM in System-Synchronous Mode**

Symbol	Description	Device	Speed Grade				Units
			-4	-3	-2	-1L	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, *with* DCM in System-Synchronous Mode.							
$T_{ICKOFDCM}$	Global Clock and OUTFF *with* DCM	XC6SLX4	N/A				ns
		XC6SLX9	N/A				ns
		XC6SLX16	N/A	4.78	5.57		ns
		XC6SLX25	N/A				ns
		XC6SLX25T				N/A	ns
		XC6SLX45	N/A	4.72	5.57		ns
		XC6SLX45T				N/A	ns
		XC6SLX75	N/A				ns
		XC6SLX75T				N/A	ns
		XC6SLX100	N/A				ns
		XC6SLX100T				N/A	ns
		XC6SLX150	N/A				ns
		XC6SLX150T				N/A	ns

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. DCM output jitter is already included in the timing calculation.

Table 62: **Global Clock Input to Output Delay With DCM in Source-Synchronous Mode**

Symbol	Description	Device	Speed Grade				Units
			-4	-3	-2	-1L	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, *with* DCM in Source-Synchronous Mode.							
$T_{ICKOFDCM\_0}$	Global Clock and OUTFF *with* DCM	XC6SLX4	N/A				ns
		XC6SLX9	N/A				ns
		XC6SLX16	N/A	5.72	6.64		ns
		XC6SLX25	N/A				ns
		XC6SLX25T				N/A	ns
		XC6SLX45	N/A	5.71	6.65		ns
		XC6SLX45T				N/A	ns
		XC6SLX75	N/A				ns
		XC6SLX75T				N/A	ns
		XC6SLX100	N/A				ns
		XC6SLX100T				N/A	ns
		XC6SLX150	N/A				ns
		XC6SLX150T				N/A	ns

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. DCM output jitter is already included in the timing calculation.

Table 63: **Global Clock Input to Output Delay With PLL in System-Synchronous Mode**

Symbol	Description	Device	Speed Grade				Units
			-4	-3	-2	-1L	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, *with* PLL in System-Synchronous Mode.							
$T_{ICKOFPLL}$	Global Clock and OUTFF *with* PLL	XC6SLX4	N/A				ns
		XC6SLX9	N/A				ns
		XC6SLX16	N/A	4.93	5.70		ns
		XC6SLX25	N/A				ns
		XC6SLX25T				N/A	ns
		XC6SLX45	N/A	5.06	5.92		ns
		XC6SLX45T				N/A	ns
		XC6SLX75	N/A				ns
		XC6SLX75T				N/A	ns
		XC6SLX100	N/A				ns
		XC6SLX100T				N/A	ns
		XC6SLX150	N/A				ns
		XC6SLX150T				N/A	ns

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. PLL output jitter is included in the timing calculation.

Table 64: **Global Clock Input to Output Delay With PLL in Source-Synchronous Mode**

Symbol	Description	Device	Speed Grade				Units
			-4	-3	-2	-1L	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, *with* PLL in Source-Synchronous Mode.							
$T_{ICKOFPLL\_0}$	Global Clock and OUTFF *with* PLL	XC6SLX4	N/A				ns
		XC6SLX9	N/A				ns
		XC6SLX16	N/A	5.92	6.89		ns
		XC6SLX25	N/A				ns
		XC6SLX25T				N/A	ns
		XC6SLX45	N/A	6.05	7.11		ns
		XC6SLX45T				N/A	ns
		XC6SLX75	N/A				ns
		XC6SLX75T				N/A	ns
		XC6SLX100	N/A				ns
		XC6SLX100T				N/A	ns
		XC6SLX150	N/A				ns
		XC6SLX150T				N/A	ns

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. PLL output jitter is included in the timing calculation.

Table 65: **Global Clock Input to Output Delay With DCM and PLL in System-Synchronous Mode**

Symbol	Description	Device	Speed Grade				Units
			-4	-3	-2	-1L	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, *with* DCM and PLL in System-Synchronous Mode.							
$T_{ICKOFDCM\_PLL}$	Global Clock and OUTFF with DCM and PLL	XC6SLX4	N/A				ns
		XC6SLX9	N/A				ns
		XC6SLX16	N/A	5.44	6.29		ns
		XC6SLX25	N/A				ns
		XC6SLX25T				N/A	ns
		XC6SLX45	N/A	5.38	6.28		ns
		XC6SLX45T				N/A	ns
		XC6SLX75	N/A				ns
		XC6SLX75T				N/A	ns
		XC6SLX100	N/A				ns
		XC6SLX100T				N/A	ns
		XC6SLX150	N/A				ns
		XC6SLX150T				N/A	ns

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. DCM and PLL output jitter are already included in the timing calculation.

Table 66: **Global Clock Input to Output Delay With DCM and PLL in Source-Synchronous Mode**

Symbol	Description	Device	Speed Grade				Units
			-4	-3	-2	-1L	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, *with* DCM and PLL in Source-Synchronous Mode.							
$T_{ICKOFDCM0\_PLL}$	Global Clock and OUTFF with DCM and PLL	XC6SLX4	N/A				ns
		XC6SLX9	N/A				ns
		XC6SLX16	N/A	6.38	7.36		ns
		XC6SLX25	N/A				ns
		XC6SLX25T				N/A	ns
		XC6SLX45	N/A	6.37	7.35		ns
		XC6SLX45T				N/A	ns
		XC6SLX75	N/A				ns
		XC6SLX75T				N/A	ns
		XC6SLX100	N/A				ns
		XC6SLX100T				N/A	ns
		XC6SLX150	N/A				ns
		XC6SLX150T				N/A	ns

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. DCM and PLL output jitter are already included in the timing calculation.

Spartan-6 Device Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. The representative values for typical pin locations and normal clock loading are listed in Table 67 through Table 73. Values are expressed in nanoseconds unless otherwise noted.

Table 67: **Global Clock Setup and Hold Without DCM or PLL**

Symbol	Description	Device	Speed Grade				Units
			-4	-3	-2	-1L	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.(1)							
T_{PSFD}/ T_{PHFD}	Full Delay (Legacy Delay or Default Delay) Global Clock and IFF(2) without DCM or PLL	XC6SLX4	N/A				ns
		XC6SLX9	N/A				ns
		XC6SLX16	N/A	2.35/ –0.01	2.85/ –0.01		ns
		XC6SLX25	N/A				ns
		XC6SLX25T				N/A	ns
		XC6SLX45	N/A	2.60/ 0.04	3.26/ 0.04		ns
		XC6SLX45T				N/A	ns
		XC6SLX75	N/A				ns
		XC6SLX75T				N/A	ns
		XC6SLX100	N/A				ns
		XC6SLX100T				N/A	ns
		XC6SLX150	N/A				ns
		XC6SLX150T				N/A	ns

Notes:
1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input Flip-Flop or Latch.

Table 68: **Global Clock Setup and Hold With DCM in System-Synchronous Mode**

Symbol	Description	Device	Speed Grade				Units
			-4	-3	-2	-1L	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.(1)							
T_{PSDCM}/ T_{PHDCM}	No Delay Global Clock and IFF(2) with DCM in System-Synchronous Mode	XC6SLX4	N/A				ns
		XC6SLX9	N/A				ns
		XC6SLX16	N/A	1.96/ 0.23	2.20/ 0.23		ns
		XC6SLX25	N/A				ns
		XC6SLX25T				N/A	ns
		XC6SLX45	N/A	2.01/ 0.18	3.24/ 0.18		ns
		XC6SLX45T				N/A	ns
		XC6SLX75	N/A				ns
		XC6SLX75T				N/A	ns
		XC6SLX100	N/A				ns
		XC6SLX100T				N/A	ns
		XC6SLX150	N/A				ns
		XC6SLX150T				N/A	ns

Notes:
1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include DCM CLK0 jitter.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 69: **Global Clock Setup and Hold With DCM in Source-Synchronous Mode**

Symbol	Description	Device	Speed Grade				Units
			-4	-3	-2	-1L	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.(1)							
T_{PSDCM0}/ T_{PHDCM0}	No Delay Global Clock and IFF(2) with DCM in Source-Synchronous Mode	XC6SLX4	N/A				ns
		XC6SLX9	N/A				ns
		XC6SLX16	N/A	1.01/ 0.77	1.11/ 0.80		ns
		XC6SLX25	N/A				ns
		XC6SLX25T				N/A	ns
		XC6SLX45	N/A	1.06/ 0.78	2.15/ 0.80		ns
		XC6SLX45T				N/A	ns
		XC6SLX75	N/A				ns
		XC6SLX75T				N/A	ns
		XC6SLX100	N/A				ns
		XC6SLX100T				N/A	ns
		XC6SLX150	N/A				ns
		XC6SLX150T				N/A	ns

Notes:
1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include DCM CLK0 jitter.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 70: **Global Clock Setup and Hold With PLL in System-Synchronous Mode**

Symbol	Description	Device	Speed Grade				Units
			-4	-3	-2	-1L	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.(1)							
T_{PSPLL}/ T_{PHPLL}	No Delay Global Clock and IFF(2) with PLL in System-Synchronous Mode	XC6SLX4	N/A				ns
		XC6SLX9	N/A				ns
		XC6SLX16	N/A	1.90/ 0.24	2.05/ 0.24		ns
		XC6SLX25	N/A				ns
		XC6SLX25T				N/A	ns
		XC6SLX45	N/A	1.68/ 0.33	1.82/ 0.33		ns
		XC6SLX45T				N/A	ns
		XC6SLX75	N/A				ns
		XC6SLX75T				N/A	ns
		XC6SLX100	N/A				ns
		XC6SLX100T				N/A	ns
		XC6SLX150	N/A				ns
		XC6SLX150T				N/A	ns

Notes:
1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include PLL CLKOUT0 jitter.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 71: **Global Clock Setup and Hold With PLL in Source-Synchronous Mode**

Symbol	Description	Device	Speed Grade				Units
			-4	-3	-2	-1L	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.(1)							
T_{PSPLL0}/ T_{PHPLL0}	No Delay Global Clock and IFF(2) with PLL in Source-Synchronous Mode	XC6SLX4	N/A				ns
		XC6SLX9	N/A				ns
		XC6SLX16	N/A	0.88/ 0.97	0.88/ 1.05		ns
		XC6SLX25	N/A				ns
		XC6SLX25T				N/A	ns
		XC6SLX45	N/A	0.66/ 1.11	0.66/ 1.26		ns
		XC6SLX45T				N/A	ns
		XC6SLX75	N/A				ns
		XC6SLX75T				N/A	ns
		XC6SLX100	N/A				ns
		XC6SLX100T				N/A	ns
		XC6SLX150	N/A				ns
		XC6SLX150T				N/A	ns

Notes:
1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include PLL CLKOUT0 jitter.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 72: **Global Clock Setup and Hold With DCM and PLL in System-Synchronous Mode**

Symbol	Description	Device	Speed Grade				Units
			-4	-3	-2	-1L	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.(1)							
$T_{PSDCMPLL}$/ $T_{PHDCMPLL}$	No Delay Global Clock and IFF(2) with DCM and PLL in System-Synchronous Mode	XC6SLX4	N/A				ns
		XC6SLX9	N/A				ns
		XC6SLX16	N/A	2.05/ 0.92	2.21/ 0.92		ns
		XC6SLX25	N/A				ns
		XC6SLX25T				N/A	ns
		XC6SLX45	N/A	1.95/ 0.87	3.21/ 0.87		ns
		XC6SLX45T				N/A	ns
		XC6SLX75	N/A				ns
		XC6SLX75T				N/A	ns
		XC6SLX100	N/A				ns
		XC6SLX100T				N/A	ns
		XC6SLX150	N/A				ns
		XC6SLX150T				N/A	ns

Notes:
1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include CMT jitter; DCM CLK0 driving PLL, PLL CLKOUT0 driving BUFG.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 73: **Global Clock Setup and Hold With DCM and PLL in Source-Synchronous Mode**

Symbol	Description	Device	Speed Grade				Units
			-4	-3	-2	-1L	
Example Data Input Set-Up and Hold Times Relative to a Forwarded Clock Input Pin,(1) Using DCM, PLL, and Global Clock Buffer. For situations where clock and data inputs conform to different standards, adjust the setup and hold values accordingly using the values shown in IOB Switching Characteristics, page 17.							
$T_{PSDCMPLL\_0}$/ $T_{PHDCMPLL\_0}$	No Delay Global Clock and IFF(2) with DCM and PLL in Source-Synchronous Mode	XC6SLX4	N/A				ns
		XC6SLX9	N/A				ns
		XC6SLX16	N/A	1.10/ 1.43	1.12/ 1.52		ns
		XC6SLX25	N/A				ns
		XC6SLX25T				N/A	ns
		XC6SLX45	N/A	1.00/ 1.44	2.12/ 1.51		ns
		XC6SLX45T				N/A	ns
		XC6SLX75	N/A				ns
		XC6SLX75T				N/A	ns
		XC6SLX100	N/A				ns
		XC6SLX100T				N/A	ns
		XC6SLX150	N/A				ns
		XC6SLX150T				N/A	ns

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. The timing values were measured using the fine-phase adjustment feature of the DCM. These measurements include CMT jitter; DCM CLK0 driving PLL, PLL CLKOUT0 driving BUFG. Package skew is not included in these measurements.
2. IFF = Input Flip-Flop

Source-Synchronous Switching Characteristics

The parameters in this section provide the necessary values for calculating timing budgets for Spartan-6 FPGA source-synchronous transmitter and receiver data-valid windows.

Table 74: **Duty Cycle Distortion and Clock-Tree Skew**

Symbol	Description	Device[1]	Speed Grade				Units
			-4	-3	-2	-1L	
T_{DCD_CLK}	Global Clock Tree Duty Cycle Distortion[2]	All	0.20	0.20	0.20		ns
T_{CKSKEW}	Global Clock Tree Skew [3]	XC6SLX4	N/A				ns
		XC6SLX9	N/A				ns
		XC6SLX16	N/A	0.15	0.15		ns
		XC6SLX25	N/A				ns
		XC6SLX25T				N/A	ns
		XC6SLX45	N/A	0.20	0.20		ns
		XC6SLX45T				N/A	ns
		XC6SLX75	N/A				ns
		XC6SLX75T				N/A	ns
		XC6SLX100	N/A				ns
		XC6SLX100T				N/A	ns
		XC6SLX150	N/A				ns
		XC6SLX150T				N/A	ns
T_{DCD_BUFIO2}	I/O clock tree duty cycle distortion	All	0.25	0.25	0.25		ns
$T_{BUFIOSKEW}$	I/O clock tree skew across one clock region	XC6SLX4					ns
		XC6SLX9					ns
		XC6SLX16		0.06	0.06		ns
		XC6SLX25					ns
		XC6SLX25T					ns
		XC6SLX45		0.06	0.06		ns
		XC6SLX45T					ns
		XC6SLX75					ns
		XC6SLX75T					ns
		XC6SLX100					ns
		XC6SLX100T					ns
		XC6SLX150					ns
		XC6SLX150T					ns

Notes:

1. LX devices are not available with a -4 speed grade; LXT devices are not available with a -1L speed grade.
2. These parameters represent the worst-case duty cycle distortion observable at the pins of the device using LVDS output buffers. For cases where other I/O standards are used, IBIS can be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times.
3. The T_{CKSKEW} value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx FPGA Editor and Timing Analyzer tools to evaluate clock skew specific to your application.

Table 75: **Package Skew**

Symbol	Description	Device	Package(3)	Value	Units
$T_{PKGSKEW}$	Package Skew(1)	XC6SLX4	TQG144		ps
			CPG196		ps
			CSG225		ps
		XC6SLX9	TQG144		ps
			CPG196		ps
			CSG225		ps
			FT(G)256		ps
			CSG324		ps
		XC6SLX16	CPG196	20	ps
			CSG225	80	ps
			FT(G)256	77	ps
			CSG324	54	ps
		XC6SLX25	FT(G)256		ps
			CSG324		ps
			FG(G)484		ps
		XC6SLX25T	CSG324		ps
			FG(G)484		ps
		XC6SLX45	CSG324	84	ps
			CSG484	106	ps
			FG(G)484	115	ps
			FG(G)676		ps
		XC6SLX45T	CSG324	56	ps
			CSG484	135	ps
			FG(G)484	84	ps
		XC6SLX75	CSG484		ps
			FG(G)484		ps
			FG(G)676		ps
		XC6SLX75T	CSG484		ps
			FG(G)484		ps
			FG(G)676		ps
		XC6SLX100	CSG484		ps
			FG(G)484		ps
			FG(G)676		ps
		XC6SLX100T	CSG484		ps
			FG(G)484		ps
			FG(G)676		ps
			FG(G)900		ps

Table 75: **Package Skew *(Cont'd)***

Symbol	Description	Device	Package(3)	Value	Units
$T_{PKGSKEW}$	Package Skew(1)	XC6SLX150	CSG484	90	ps
			FG(G)484	99	ps
			FG(G)676	97	ps
			FG(G)900	105	ps
		XC6SLX150T	CSG484	86	ps
			FG(G)484	70	ps
			FG(G)676	150	ps
			FG(G)900	104	ps

Notes:
1. These values represent the worst-case skew between any two SelectIO resources in the package: shortest delay to longest delay from Pad to Ball.
2. Package delay information is available for these device/package combinations. This information can be used to deskew the package.
3. Some of these devices are available in both Pb and Pb-free (additional G) packages as standard ordering options.

Table 76: **Sample Window**

Symbol	Description	Device(1)	Speed Grade				Units
			-4	-3	-2	-1L	
T_{SAMP}	Sampling Error at Receiver Pins(2)	All	510	510	560		ps
T_{SAMP_BUFIO2}	Sampling Error at Receiver Pins using BUFIO2(3)	All	430	430	480		ps

Notes:
1. LX devices are not available with a -4 speed grade; LXT devices are not available with a -1L speed grade.
2. This parameter indicates the total sampling error of Spartan-6 FPGA DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the DCM to capture the DDR input registers' edges of operation. These measurements include:
   - CLK0 DCM jitter
   - DCM accuracy (phase offset)
   - DCM phase shift resolution

   These measurements do not include package or clock tree skew.
3. This parameter indicates the total sampling error of Spartan-6 FPGA DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the BUFIO2 clock network and IODELAY to capture the DDR input registers' edges of operation. These measurements do not include package or clock tree skew.

Table 77: **Source-Synchronous Pin-to-Pin Setup/Hold and Clock-to-Out Using BUFIO2**

Symbol	Description	Device	Speed Grade				Units
			-4	-3	-2	-1L	
Data Input Setup and Hold Times Relative to a Forwarded Clock Input Pin Using BUFIO2							
T_{PSCS}/T_{PHCS}	IFF setup/hold using BUFIO2 clock	XC6SLX4	N/A				ns
		XC6SLX9	N/A				ns
		XC6SLX16	N/A	0.55/ 0.75	0.70/ 0.82		ns
		XC6SLX25	N/A				ns
		XC6SLX25T					ns
		XC6SLX45	N/A	0.44/ 1.23	0.50/ 1.37		ns
		XC6SLX45T				N/A	ns
		XC6SLX75	N/A				ns
		XC6SLX75T				N/A	ns
		XC6SLX100	N/A				ns
		XC6SLX100T				N/A	ns
		XC6SLX150	N/A				ns
		XC6SLX150T				N/A	ns
Pin-to-Pin Clock-to-Out Using BUFIO2							
$T_{ICKOFCS}$	OFF clock-to-out using BUFIO2 clock	XC6SLX4	N/A				ns
		XC6SLX9	N/A				ns
		XC6SLX16	N/A	5.70	6.67		ns
		XC6SLX25	N/A				ns
		XC6SLX25T					ns
		XC6SLX45	N/A	6.16	7.22		ns
		XC6SLX45T				N/A	ns
		XC6SLX75	N/A				ns
		XC6SLX75T				N/A	ns
		XC6SLX100	N/A				ns
		XC6SLX100T				N/A	ns
		XC6SLX150	N/A				ns
		XC6SLX150T				N/A	ns

Revision History

The following table shows the revision history for this document.

Date	Version	Description of Revisions
06/24/09	1.0	Initial Xilinx release.
08/26/09	1.1	Added V_{FS} to Table 1and Table 2. Added R_{FUSE} to Table 2. Added XC6SLX75 and XC6SLX75T to V_{BATT} and I_{BATT} in Table 1, Table 2, and Table 3. Corrected the quiescent supply current for the XC6SLX4 in Table 4. Updated Table 10. Removed DV_{PPIN} from Figure 2. Removed $F_{PCIECORE}$ from Table 23 and added values to $F_{PCIEUSER}$. Added more networking applications to Table 24. Updated values for $T_{SUSPENDLOW\_AWAKE}$, $T_{SUSPEND\_ENABLE}$, and T_{SCP_AWAKE} in Table 44. Numerous changes to Table 45, page 42 including the addition of new values to various specifications, revising the $T_{SMCKCSO}$ description, and changing the units of T_{POR}. Also, removed *Dynamic Reconfiguration Port (DRP) for DCM and PLL Before and After DCLK section* from Table 45 and updated all the notes. In Table 49, added to F_{INMAX}, revised F_{OUTMAX}, and removed PLL Maximum Output Frequency for BUFIO2. Revised values for DCM_DELAY_STEP in Table 51. Updated CLKIN_FREQ_FX values in Table 52.
01/04/10	1.2	Added -4 speed grade to entire document. Updated speed specification of -4, -3, -2 speed grades to version 1.03. Added -1L speed grade numbers per speed specification 1.00. Updated T_{SOL} in Table 1. Added -1L rows for LVCMOS12, LVCMOS15, and LVCMOS18 in Table 8. Revised much of the detail in GTP Transceiver Specifications in Table 11 through Table 22. Added -2 data to Table 24. Updated F_{MAX} in Table 42. Updated descriptions for $T_{DNACLKL}$ and $T_{DNACLKH}$ in Table 43 and revised values for all parameters. Removed $T_{INITADDR}$ from Table 45 and added new data. Updated values in Table 46 through Table 59. Added Table 48 (BUFPLL) and Table 54 (DCM_CLKGEN). Removed $T_{LOCKMAX}$ note from Table 49. Updated note 3 in Table 50. In Table 75: removed XC6SLX75CSG324 and XC6SLX75TCSG324; added XC6SLX75FG(G)484 and XC6SLX75FG(G)484.
02/22/10	1.3	Production release of XC6SLX16 -2 speed grade devices. The changes to Table 25 and Table 26 includes updating this data sheet to the data in ISE v11.5 software with speed specification v1.06. Updated maximum of V_{IN} and V_{TS} and note 2 in Table 1. In Table 2, changed V_{IN}, added I_{IN} and note 5, revised notes 1, 6, and 7, and added note 8 to R_{FUSE}. In Table 3, removed previous note 1 and added data to I_{RPU}, I_{RPD}, and I_{BATT}, changed C_{IN}, added R_{DT} and R_{IN_TERM}, and added note 2 and 3. Updated V_{CCO2} in Table 5. Added Table 6 and Table 7. Removed PCI66_3 from Table 8. Updated PCI33_3 and I2C in Table 8. Updated the description of Table 10. Completely updated Table 24. Updated Table 27 including adding values for PCI33_3. Updated V_{REF} value for HSTL_III_18 in Table 29. Updates missing V_{REF} values in Table 30. Added Simultaneously Switching Outputs, page 26. Removed T_{GSRQ} and T_{RPW} from Table 33 and Table 34. Also removed T_{DOQ} from Table 34. Removed T_{ISDO_DO} and note 1 from Table 35. Removed T_{OSCCK_S} and combinatorial section from Table 36. In Table 37, removed T_{IODDO_T} and added new tap parameters and note 2. In Table 38, Table 39, and Table 40, made typographical edits and removed notes. Removed clock CLK section in Table 39. Removed clock CLK section and T_{REG_MUX} and T_{REG_M31} in Table 40. Added block RAM F_{MAX} values to Table 41. Updated values and added note 2 to Table 43. Added values to Table 44 and removed note 1. Numerous changes to Table 45. Completely updated Table 54. Revised data in Table 59. Removed note 3 from Table 67. Added values to Table 75. Added data to Table 76 and Table 77.
03/10/10	1.4	Production release of XC6SLX45 -2 speed grade devices, which includes changes to Table 25 and Table 26 updating this data sheet to the data in ISE v11.5 software with speed specification v1.07. Fixed R_{IN_TERM} description in Table 3. Added PCI66_3 to Table 6 and replaced note 1. Corrected note 1 and the V, Max for TMDS_33 in Table 7. In Table 9, added note 1 to LVPECL_33 and TMDS_33. Also updated specifications for TMDS_33. Updated the GTP Transceiver Specifications section including adding values to Table 15, Table 16, and Table 19 through Table 22. Added PCI66_3 back into Table 8, Table 27, Table 29, Table 30, and Table 32. Updated note 3 on Table 30. In Table 32, corrected some typographical errors and fixed SSO limits for bank1/3 in FG(G)484 package. Corrected T_{OSCKC_OCE} in Table 36. In Table 54, updated CLKFX_FREEZE_VAR and CLKFX_FREEZE_TEMP_SLOPE and added typical values to $T_{CENTER\_LOW\_SPREAD}$ and $T_{CENTER\_HIGH\_SPREAD}$. Updated and added values to Table 60 through Table 74, and Table 77. In Table 75, revised the XC6SLX16-CSG324 and the XC6SLX45-CSG484 and FG(G)484 values.

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